Project : Insertion Demonstrations of Digital Gallium Arsenide

CDRL Item A001

OBP-80 FINAL TECHNICAL REPORT

Volume 2/4 - Source Control Drawings

Prepared for:

Naval Research Laboratories
Space Systems Division
4555 Overlook Avenue
Washington, DC. 20375

Prepared By:

Martin Marietta Space Systems
Technical Operations
P.O. Box 179
Denver, Colorado 80201

GLOSSARY

AALU	Address Arithmetic Logic Unit
ALU	Arithmetic Logic Unit
APG	Automatic Pattern Generation
ASIC	Application Specific Integrated Circuit
BCU	Bus Control Unit
BLM	Behavioral Language Model
CB	Communications Buffer
CDR	Critical Design Review
CMOS	Complementary Metal Oxide Semiconductor
CMOS/SOS	Complementary Metal Oxide Semiconductor/Silicon on Sapphire
CPU	Central Processing Unit
DALU	Data Arithmetic Logic Unit
DARPA	Defense Advanced Research Projects Administration
DC	Direct Current
DMSP	Defense Meteorological Satellite Program
DSP	Digital Signal Processing
FET	Field Effect Transistor
FIFO	First In First Out
FMEA	Failure Mode Effects Analysis
EDM	Engineering Development Model
GALU	Generic Arithmetic Logic Unit
GaAs	Gallium Arsenide
GTE	Ground Test Equipment
GFP	Government Furnished Property
I/O	Input/Output
IR&D	Independent Research and Development
MCS	Microcode Sequencer
MESFET	Metal Semiconductor Field Effect Transistor
MOPS	Million Operations Per Second
MOS	Metal Oxide Semiconductor
MPY	Multiplier Unit
MTBF	Mean Time Between Failures
NMOS	N channel Metal Oxide Semiconductor
NRL	Naval Research Laboratory
OBP	On Board Processor
OBP-80	On Board Processor - 80 MHz
OTS	Off The Shelf
PC	Personal Computer
PCA	Parts Characterization Analyzer
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PIC	Priority Interrupt Controller
PS	Pipeline Slice
Qc	Critical Charge

RAM	Random Access Memory
SEU	Single Event Upset
SSI	Small Scale Integration
TMA	Timing Margin Analysis
TTL	Transistor - Transistor Logic
VLSI	Very Large Scale Integration
WBS	Work Breakdown Structure
WCA	Worst Case Analysis
WCS	Writable Control Store
WS	Working Store

FOREWORD

The OBP-80 is an Engineering Development Model (EDM) of a bit slice computer constructed by Martin Marietta Space Systems for the Naval Research Laboratory. The work described in this report was performed under contract N00014-89-C-2169, Insertion Demonstrations of Digital Gallium Arsenide - OBP Upgrade. The contract was performed in cooperation with the Defense Advanced Research Projects Agency technology insertion program for digital gallium arsenide.

This system has been developed to demonstrate, in a laboratory environment, an architecture that can be used to perform advanced signal processing functions onboard a spacecraft. Primary emphasis is placed on the transfer of an existing CMOS architecture to a higher performance, more radiation tolerant technology of Gallium Arsenide.

The following individuals provided technical direction and assistance:

Dr. Andrew J. Fox, Head, Advanced Systems Technology Branch, NRL
Dr. Arati Prabhakar, Director, Defense Sciences Office, DARPA
Dr. Alan Ross, Architecture Consultant

IDDGA Final Technical Report Volume 2 of 4 contains the Source Control Drawings for the GaAs VLSI chip set.

This volume provides the procurement specification for the 'Class B' military versions of all seven VLSI components used in the OBP-80 EDM. The SCD identifies pattern numbers, DC and AC parameteric tests, and required burn in circuitry. This data is provided to facilitate component procurement for the flight devices.

The complete final technical report is composed of the following volumes:

Final Technical Report - Volume 1 of 4: Chip Set Schematic Diagrams

Final Technical Report - Volume 2 of 4: Chip Set Source Control Drawings

Final Technical Report - Volume 3 of 4: EDM Board Schematic Diagrams

Final Technical Report - Volume 4 of 4: OBP80 Software Model

1. INTRODUCTION

The OBP80 chip set is composed of the following circuits:

TABLE 1 OBP80 Chip Set Summary

DEVICE	PACKAGE	TRANSISTOR COUNT	EQUIVALENT GATES	POWER	I/O	MASK REVISION
GOBP001 - MPY VLSI	LDCC 256	27,105	9,035	3.35 W	43 GND, 27 VTT, 136 GaAs signal	Rev. A 7/15/91
GOBP002 - GALU VLSI	LDCC 344	73,564	24,521	6.6 W	80 GND, 36 VTT, 214 GaAs signal	Initial 3/15/91
GOBP003 - IPR VLSI	LDCC 344	26,600	8,867	4.4 W	64 GND,24 VTT,5 VREF, 112 ECL signal, 136 GaAs signal	Rev. A 7/30/91
GOBP004 - DMC VLSI	LDCC 344	14,887	4,962	2.95 W	77 GND,31 VTT,4 VREF, 102 ECL signal, 105 GaAs signal	Initial 3/15/91
GOBP005 - TICVLSI	LDCC 256	14,750	4,916			Initial 7/30/91
GOBP006 - COMM1 VLSI	LDCC 256	15,780	5,260		41 GND, 26 VTT, 15 PLUS5, 92 GaAs signal, 81 TTL signal	Initial 7/15/91
GOBP007 MCS VLSI	LDCC 344	37,094	12,364			Initial 8/15/91

The table above illustrates that there are a variety of voltage interface standards used in the OBP80 VLSI chip set. The voltage standards are required for interoperability with other standard components, inluding the WCS and WS RAM devices as well as the OBP backplane specification. The paramteric tests identified in this document are specifically tailored for each unique voltage interface standard.

It should be remembered that all OBP80 VLSI componets developed in E/D mode MESFET GaAs technology derive their voltage reference from the -2.0 V supply. Therefore, the threshold voltage of the GaAs device will vary millivolt for millivolt with the VTT supply voltage, regardless of the interface standard. It was impossible to develop threshold voltages from the local ground reference, due to the formation of sneak paths developing in the power strobing situation.

Figure 1 illustrates the significance of this. The figure shows that the -2V supply is generated in the usual manner, and produces an output voltage that has a 10% tolerance with respect to the local ground. This implies that the voltage measured on the -2V plane will range between -1.8 V and -2.2 V with respect to the local ground.

This might lead one to correctly assume that the GaAs components should be designed and specified such that the I/O parameters withstand a 10% variation in the -2V power supply. The technology is extremely tolerant of variations in operating voltage span. For instance, many of the GaAs components will function well with only 1 Volt of potential between VTT and ground.

However, the technology is very intolerant of variations in the local VTT reference. An example 'worst case' condition might be to assume that the receiver VTT supply is at -2.2 volts, while the driver VTT supply is at -1.8 volts. This would introduce a 400 mV reduction in noise margins.

To compensate for this condition, the GaAs voltage interface standard has been expanded by 500 mV over the ECL 100K specification. This allows the GaAs componets to be specified in the conventional manner. However, the GaAs components are not approved for usage in such a manner. The specification for the OBP80 chip set shall include the following limitations.:

1. The ECL and GaAs interface specifications are designed for local connection only. Specifically, the GaAs interface voltage specification shall not be utilized for PWB - PWB connections, or in any design situation involving connectors.

2. Any GaAs VLSI devices exhibiting connections utilizing the GaAs or ECL interface voltage standard shall derive power and voltage reference from the same supply source(s).

3. Any physical package design utilizing GaAs VLSI components shall supply a VTT reference that provides less than 10 milliohms of resistance and less than 10 nH of inductance between any VTT pin of any GaAs VLSI device. These two specifications each consume 200 mV of noise immunity for a chip set requiring 20 A of DC current and providing 16 mA of current into a rise time of 800 pS.

It should be noted that the TTL and GaAs interface circuits are of the 'Push-Pull' variety. The GaAs VLSI components employ large numbers of these devices. Conventional wafer probe technology designed for large pincount VLSI is not sufficient to test these circuits due to the inability to meet the specification of (3.) above. In such cases, the SCD provides relaxation of the test specification in the form of enlarged input voltage swings. This is intended to facilitate selection of functional devices for packaging. This relaxation does not apply to finished, packaged devices.

2. Voltage Interface Specifications for GaAs VLSI Components

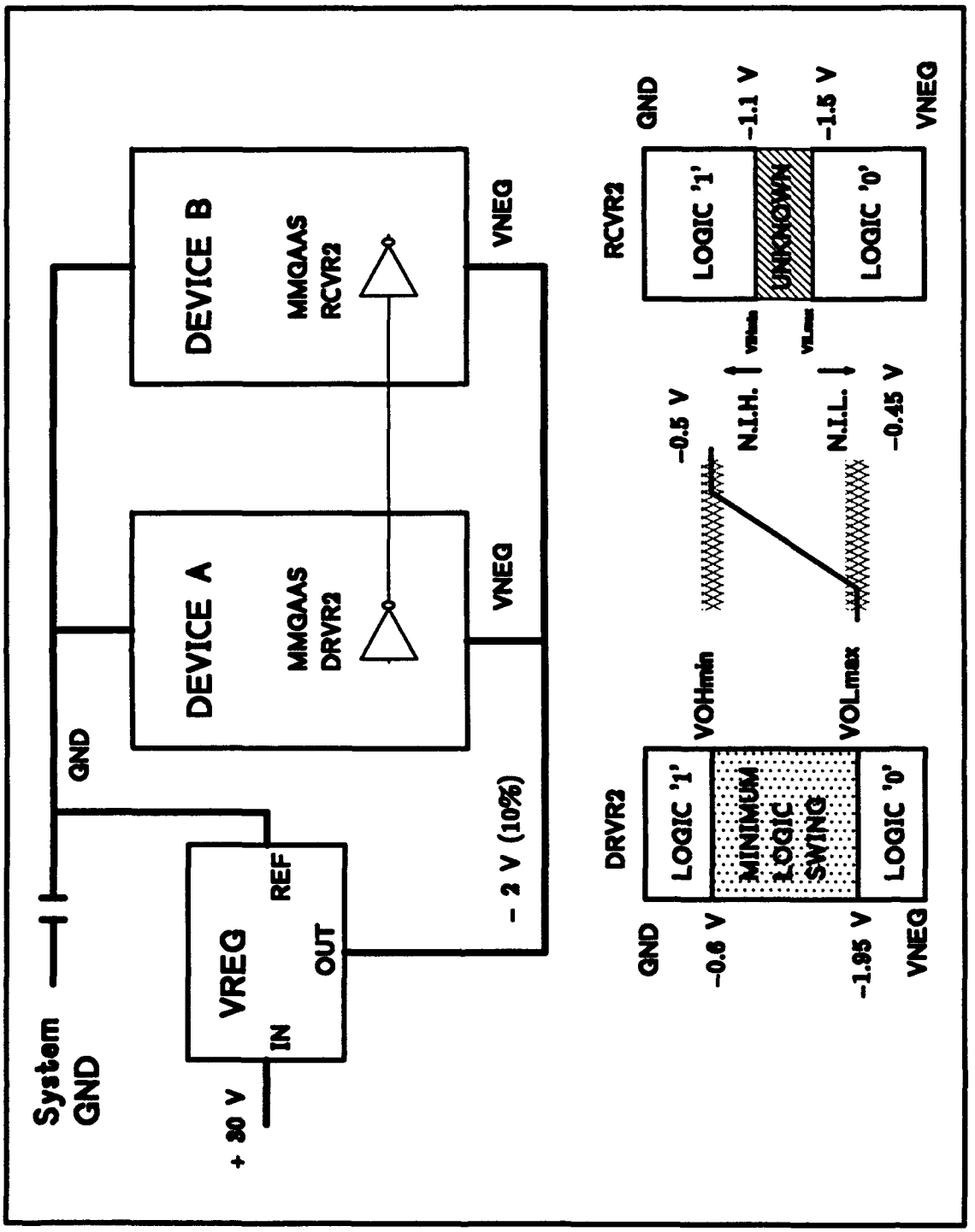

Figure 1 Approved GaAs Interface Environment

GaAs Input Interface Standard:

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

3. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

4. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

GaAs Output Interface Standard:

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

3. VOH ECL -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -1.020 V when the test is performed with the following parametric conditions:

   Vin=Vih(max) or Vil(min)

4. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

5. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

6. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

7. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

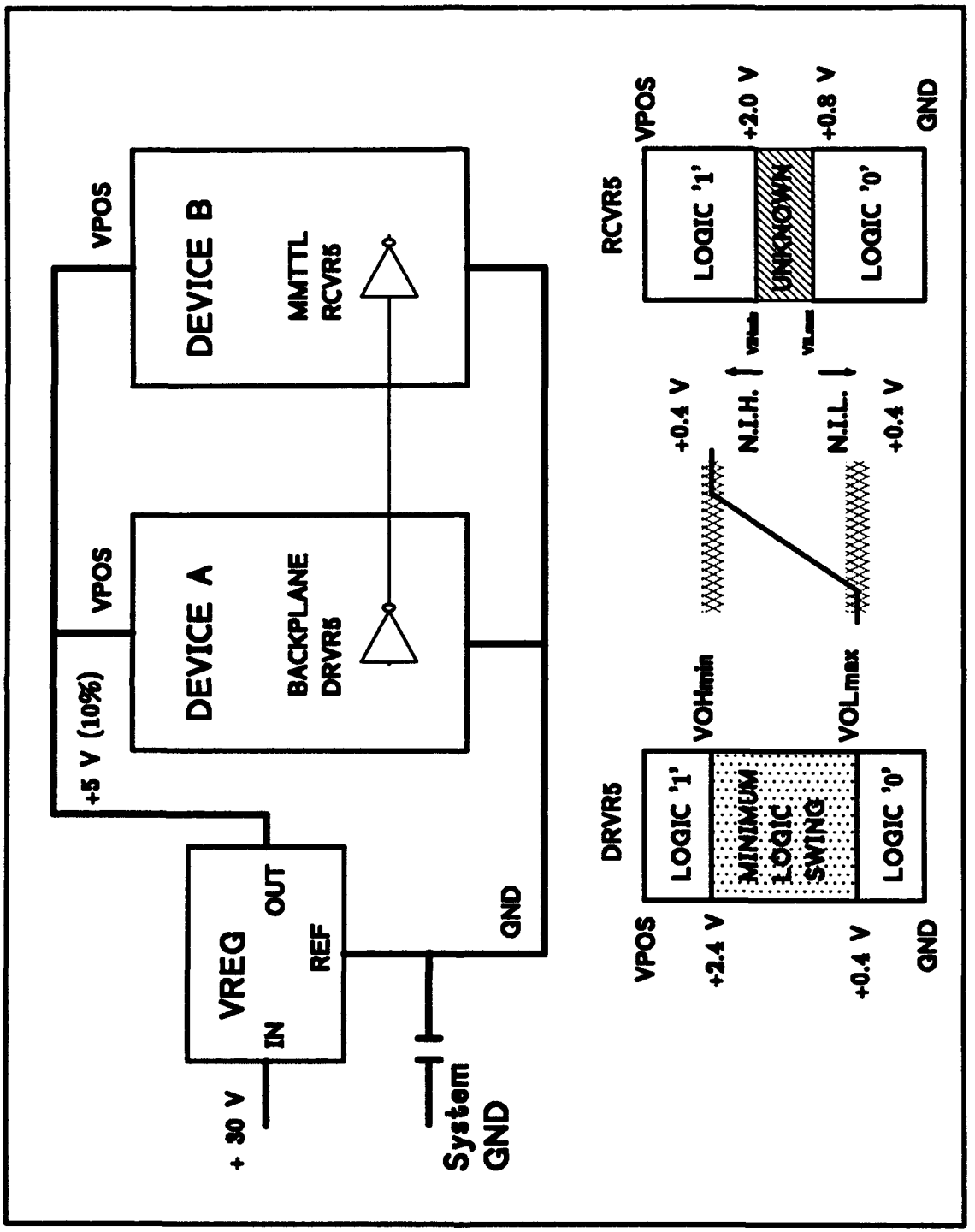

Figure 2 Approved TTL Interface Environment

TTL Input Interface Standard:

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = +2.0 V.

2. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = +0.8 V.

3. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = +2.4 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

4. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = 0.4 V, VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = = VCC = PLUS5 = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

TTL Output Interface Standard:

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = +0.4 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into device pin, VTT = -1.9 V, VCCA = VCC = 0 V, PLUS5 =5.5 V.

2. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = +2.4 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into device pin, VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 4.5 V.

3. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

4. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

5. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = +0.4 V, VTT = -1.9 V, VCCA = VCC = 0 V, PLUS5 = +4.5 V.

6. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = +2.4 V, VCCA = VCC = 0 V, PLUS5 = +5.5 V.

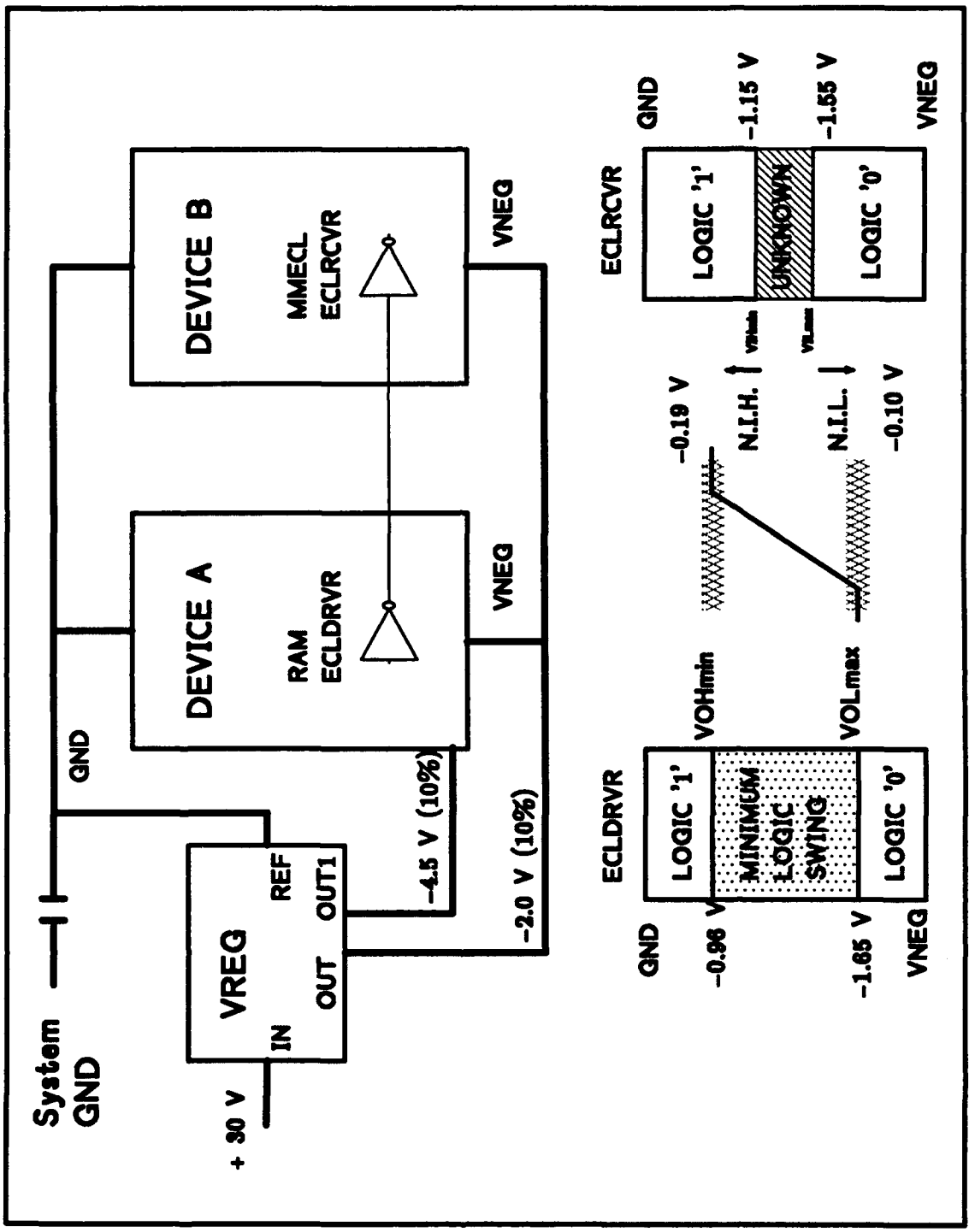

Figure 3 Approved ECL Interface Environment

ECL Input Interface Standard:

1. VIH ECL 100K -- The ECL Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.2 V

2. VIL ECL 100K -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

3. IIH ECL 100K -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

4. IIL ECL 100K -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N ECL 100K -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P ECL 100K -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

ECL Output Interface Standard:

1. VOL ECL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.620 V when the test is performed with the following parametric conditions:

   Vin=Vih(max) or Vil(min)

2. VCD1P ECL -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

3. IOSH ECL -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -50 mA when the test is performed with the following parametric conditions:

VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

Drawing Number: GOBP001

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. Sheet 0 shall not be furnished to supplier.
2. The 'Dash 2' configuration refers to the initial wafer run for design characterization only.
3. Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.

PROGRAM AUTHORIZATION
Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION
Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Principal Design Engineer

Full Custom Multiplier Device for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP001	C
SCALE	PAGE	SHEET 0 of 36

Drawing Number: GOBP001

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	10/19/90	
A	Revision A – Pattern GOBP001–MT1	11/19/90	
B	Revision B – DC Parametric Limits	12/23/90	
C	Revision C – Burn In Circuit	2/11/91	

											REV
								36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
						B	B		C		REV
22	21	20	19	18	17	16	15	14	13	12	SH
C	C										REV
11	10	9	8	7	6	5	4	3	2	1	SH

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Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION

Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Principal Design Engineer

Full Custom Multiplier Device for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP001	C
SCALE	PAGE	SHEET 1 of 36

Drawing Number: GOBP001

REVISIONS

REV	SH	DESCRIPTION	DATE	APPROVED
A	--	Altered 'Wave.t' for signal format: <signal>:B	11/19/90	
A	--	Changed pattern set signal "test" to "TST" for Teradyne keyword.	11/19/90	
A	--	Added signal "CLKN" to pattern set to drive differential clock.	11/19/90	
B	13	Modified 4.3 to include device loading during functional test.	12/23/90	
B	15	Added VIH and VIL criteria. Modified VCD1N test to reflect IOL = -3.0 mA.	12/23/90	
B	16	Modified VCD1N test to reflect IOL = -3.0 mA. Modified VCD1P test to reflect IOH = 3.0 mA.	12/23/90	
C	10	Changed *radiation* specification to specify process characteristics instead of device parametrics.	2/11/91	
C	11	Added requirement for power cycling the static burn-in.	2/11/91	
C	13	Revised package acceleration test procedure from 883C, Meth. 2001 Cond. E to Cond. B.	2/11/91	

FSCM NO. 04236

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A	GOBP001	C
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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom MPY VLSI; hereinafter referred to as GOBP001, MPY, or part.

1.2 Part Number - The MPY VLSI shall be identified by the part number GOBP001.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Free-air Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP001-MT1	Magnetic media functional description of MPY VLSI
GOBP001-MT2	Magnetic media graphical description of MPY VLSI
GOBP001-MT3	Magnetic media assembly drawing of MPY VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the MPY VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP001-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP001-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP001-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the MPY VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the MPY VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

The MPY VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification should be manufactured in a 1.2 micron, E/D GaAs MESFET process. Upon request, the vendor shall permit on site examination of process flow documentation for the purposes of determining process impact on device radiation hardness. Martin Marietta has performed the design of the MPY VLSI such that a device fabricated in the above mentioned process will exhibit the following characteristics:

3.2.6.1 Total Dose - Exposure to 3E4 rads (Si) total dose and exhibit no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec and not exhibit sustained latchup.

3.2.6.3 Single Particle Upset - Exposure to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec and not exhibit data loss from critical storage elements.

The above characteristics have been demonstrated on a device test vehicle representative of the technology. This specification does not require re-characterization explicitly for the MPY VLSI.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP001-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP001-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The MPY VLSI shall be packaged in a 256 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP001-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B. Since the dominant failure mechanism in this technology is electromigration, the burn in should attempt to equalize stress among the circuit paths. The static burn in circuit of Figure 6-1 should be used for all screening and qualification tests. To even out the stress, the following test procedure should be used at periods of 1/4 the total test duration:

a. The burn-in chamber should be brought to room temperature with the devices under bias, and the case temperature allowed to stabilize.

b. All bias should be removed from the device, and the case tempcrature allowed to stabilize.

c. After 30 minutes of dwell time at room temperature, return the bias to the device.

d. Ramp the burn-in chamber back to test temperature. The test shall be assumed to be in progress after the device case temperature has stabilized.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP001-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP001-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of MPY VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition B, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on MPY-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 235. The pattern drivers should be connected, and forcing pattern number 235. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 280. The patterns drivers should be connected, and forcing pattern number 280. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on MPY-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

3. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

4. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on MPY-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

3. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

4. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

5. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

6. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

   In Table 5-1, the pins are listed sequentially from 1 to 256, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for MPY VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
1	VTT	--	--	--	--	--	--	--	--
2	VCC	--	--	--	--	--	--	--	--
3	DDINT(2)	210	13	Note 1	Note 1	13	210	--	--
4	DDINT(3)	214	13	Note 1	Note 1	13	214	--	--
5	SBS(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	VCCA	--	--	--	--	--	--	--	--
7	SBS(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
8	SBS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
9	SBS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
10	SBS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
11	VCCA	--	--	--	--	--	--	--	--
12	SRCMPY(15)	150	134	Note 1	Note 1	134	150	--	--
13	SRCMPY(14)	146	130	Note 1	Note 1	130	146	--	--
14	SRCMPY(13)	142	126	Note 1	Note 1	126	142	--	--
15	SRCMPY(12)	138	122	Note 1	Note 1	122	138	--	--
16	VTT	--	--	--	--	--	--	--	--
17	VCC	--	--	--	--	--	--	--	--
18	VCCA	--	--	--	--	--	--	--	--
19	SRCMPY(11)	150	134	Note 1	Note 1	134	150	--	--
20	SRCMPY(10)	146	130	Note 1	Note 1	130	146	--	--
21	SRCMPY(9)	142	126	Note 1	Note 1	126	142	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
22	SRCMPY(8)	138	122	Note 1	Note 1	122	138	--	--
23	CLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
24	VCCA	--	--	--	--	--	--	--	--
25	CLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
26	SRCMPY(7)	150	134	Note 1	Note 1	134	150	--	--
27	SRCMPY(6)	146	130	Note 1	Note 1	130	146	--	--
28	SRCMPY(5)	142	126	Note 1	Note 1	126	142	--	--
29	VCCA	--	--	--	--	--	--	--	--
30	SRCMPY(4)	138	122	Note 1	Note 1	122	138	--	--
31	SRCMPY(3)	150	134	Note 1	Note 1	134	150	--	--
32	VTT	--	--	--	--	--	--	--	--
33	VCC	--	--	--	--	--	--	--	--
34	SRCMPY(2)	146	130	Note 1	Note 1	130	146	--	--
35	SRCMPY(1)	142	126	Note 1	Note 1	126	142	--	--
36	VCCA	--	--	--	--	--	--	--	--
37	SRCMPY(0)	138	122	Note 1	Note 1	122	138	--	--
38	PEZ	195	27	Note 1	Note 1	27	195	--	--
39	SBI(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
40	SBI(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
41	VCCA	--	--	--	--	--	--	--	--
42	SBI(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
43	SBI(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
44	SBI(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
45	ALUCC(0)	175	159	Note 1	Note 1	159	175	--	--
46	ALUCC(1)	179	163	Note 1	Note 1	163	179	--	--
47	VCCA	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	VCC	--	--	--	--	--	--	--	--
50	ALUCC(2)	183	167	Note 1	Note 1	167	183	--	--
51	ALUCC(3)	187	171	Note 1	Note 1	171	187	--	--
52	ALUCC(4)	175	159	Note 1	Note 1	159	175	--	--
53	ALUCC(5)	179	163	Note 1	Note 1	163	179	--	--
54	VCCA	--	--	--	--	--	--	--	--
55	ALUCC(6)	183	167	Note 1	Note 1	167	183	--	--
56	ALUCC(7)	187	171	Note 1	Note 1	171	187	--	--
57	TEST	10	232	Note 1	Note 1	232	10	--	--
58	VCCA	--	--	--	--	--	--	--	--
59	VCCA	--	--	--	--	--	--	--	--
60	GND1	--	--	--	--	--	--	--	--
61	GND1	--	--	--	--	--	--	--	--
62	GND1	--	--	--	--	--	--	--	--
63	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
64	VCC	--	--	--	--	--	--	--	--
65	GND1	--	--	--	--	--	--	--	--
66	GND1	--	--	--	--	--	--	--	--
67	GND1	--	--	--	--	--	--	--	--
68	VCCA	--	--	--	--	--	--	--	--
69	VTT	--	--	--	--	--	--	--	--
70	VCC	--	--	--	--	--	--	--	--
71	GND1	--	--	--	--	--	--	--	--
72	GND1	--	--	--	--	--	--	--	--
73	VTT	--	--	--	--	--	--	--	--
74	GND1	--	--	--	--	--	--	--	--
75	GND1	--	--	--	--	--	--	--	--
76	GND1	--	--	--	--	--	--	--	--
77	GND1	--	--	--	--	--	--	--	--
78	VTT	--	--	--	--	--	--	--	--
79	VTT	--	--	--	--	--	--	--	--
80	GND1	--	--	--	--	--	--	--	--
81	GND1	--	--	--	--	--	--	--	--
82	GND1	--	--	--	--	--	--	--	--
83	GND1	--	--	--	--	--	--	--	--
84	GND1	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
85	GND1	--	--	--	--	--	--	--	--
86	GND1	--	--	--	--	--	--	--	--
87	VTT	--	--	--	--	--	--	--	--
88	VCC	--	--	--	--	--	--	--	--
89	GND1	--	--	--	--	--	--	--	--
90	GND1	--	--	--	--	--	--	--	--
91	GND1	--	--	--	--	--	--	--	--
92	GND1	--	--	--	--	--	--	--	--
93	GND1	--	--	--	--	--	--	--	--
94	GND1	--	--	--	--	--	--	--	--
95	GND1	--	--	--	--	--	--	--	--
96	GND1	--	--	--	--	--	--	--	--
97	GND1	--	--	--	--	--	--	--	--
98	VTT	--	--	--	--	--	--	--	--
99	VTT	--	--	--	--	--	--	--	--
100	VTT	--	--	--	--	--	--	--	--
101	VTT	--	--	--	--	--	--	--	--
102	GND1	--	--	--	--	--	--	--	--
103	GND1	--	--	--	--	--	--	--	--
104	GND1	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
105	SEAL RING VTT	--	--	--	--	--	--	--	--
106	VCC	--	--	--	--	--	--	--	--
107	GND1	--	--	--	--	--	--	--	--
108	GND1	--	--	--	--	--	--	--	--
109	GND1	--	--	--	--	--	--	--	--
110	GND1	--	--	--	--	--	--	--	--
111	GND1	--	--	--	--	--	--	--	--
112	GND1	--	--	--	--	--	--	--	--
113	GND1	--	--	--	--	--	--	--	--
114	GND1	--	--	--	--	--	--	--	--
115	GND1	--	--	--	--	--	--	--	--
116	GND1	--	--	--	--	--	--	--	--
117	GND1	--	--	--	--	--	--	--	--
118	GND1	--	--	--	--	--	--	--	--
119	VTT	--	--	--	--	--	--	--	--
120	VTT	--	--	--	--	--	--	--	--
121	GND1	--	--	--	--	--	--	--	--
122	GND1	--	--	--	--	--	--	--	--
123	VTT	--	--	--	--	--	--	--	--
124	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
125	VCCA	--	--	--	--	--	--	--	--
126	GND1	--	--	--	--	--	--	--	--
127	CTRL1(13)	35	19	Note 1	Note 1	19	35	--	--
128	CTRL2(13)	71	55	Note 1	Note 1	55	71	--	--
129	VTT	--	--	--	--	--	--	--	--
130	VCC	--	--	--	--	--	--	--	--
131	CTRL3(13)	107	91	Note 1	Note 1	91	107	--	--
132	CTRL1(0)	31	15	Note 1	Note 1	15	31	--	--
133	CTRL2(0)	67	51	Note 1	Note 1	51	67	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	CTRL3(0)	103	87	Note 1	Note 1	87	103	--	--
136	CTRL1(9)	35	19	Note 1	Note 1	19	35	--	--
137	CTRL2(9)	71	55	Note 1	Note 1	55	71	--	--
138	CTRL3(9)	107	91	Note 1	Note 1	91	107	--	--
139	VCCA	--	--	--	--	--	--	--	--
140	CTRL1(1)	35	19	Note 1	Note 1	19	35	--	--
141	CTRL2(1)	71	55	Note 1	Note 1	55	71	--	--
142	CTRL3(1)	107	91	Note 1	Note 1	91	107	--	--
143	CTRL1(10)	39	23	Note 1	Note 1	23	39	--	--
144	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
145	VCC	--	--	--	--	--	--	--	--
146	VCCA	--	--	--	--	--	--	--	--
147	CTRL2(10)	75	59	Note 1	Note 1	59	75	--	--
148	CTRL3(10)	111	95	Note 1	Note 1	95	111	--	--
149	CTRL1(2)	39	23	Note 1	Note 1	23	39	--	--
150	CTRL2(2)	75	59	Note 1	Note 1	59	75	--	--
151	CTRL3(2)	111	95	Note 1	Note 1	95	111	--	--
152	VCCA	--	--	--	--	--	--	--	--
153	CTRL1(11)	43	27	Note 1	Note 1	27	43	--	--
154	CTRL2(11)	79	63	Note 1	Note 1	63	79	--	--
155	CTRL3(11)	115	99	Note 1	Note 1	99	115	--	--
156	CTRL1(3)	43	27	Note 1	Note 1	27	43	--	--
157	VCCA	--	--	--	--	--	--	--	--
158	CTRL2(3)	79	63	Note 1	Note 1	63	79	--	--
159	CTRL3(3)	115	99	Note 1	Note 1	99	115	--	--
160	VTT	--	--	--	--	--	--	--	--
161	VCC	--	--	--	--	--	--	--	--
162	CTRL1(12)	31	15	Note 1	Note 1	15	31	--	--
163	CTRL2(12)	67	51	Note 1	Note 1	51	67	--	--
164	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
165	CTRL3(12)	103	87	Note 1	Note 1	87	103	--	--
166	CTRL1(4)	31	15	Note 1	Note 1	15	31	--	--
167	CTRL2(4)	67	51	Note 1	Note 1	51	67	--	--
168	CTRL3(4)	103	87	Note 1	Note 1	87	103	--	--
169	VCCA	--	--	--	--	--	--	--	--
170	CTRL1(8)	31	15	Note 1	Note 1	15	31	--	--
171	CTRL2(8)	67	51	Note 1	Note 1	51	67	--	--
172	CTRL3(8)	103	87	Note 1	Note 1	87	103	--	--
173	CTRL1(5)	35	19	Note 1	Note 1	19	35	--	--
174	CTRL2(5)	71	55	Note 1	Note 1	55	71	--	--
175	VCCA	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--
177	VCC	--	--	--	--	--	--	--	--
178	CTRL3(5)	107	91	Note 1	Note 1	91	107	--	--
179	CTRL1(14)	39	23	Note 1	Note 1	23	39	--	--
180	CTRL2(14)	75	59	Note 1	Note 1	59	75	--	--
181	CTRL3(14)	111	95	Note 1	Note 1	95	111	--	--
182	VCCA	--	--	--	--	--	--	--	--
183	CTRL1(6)	39	23	Note 1	Note 1	23	39	--	--
184	CTRL2(6)	75	59	Note 1	Note 1	59	75	--	--

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
185	CTRL3(6)	111	95	Note 1	Note 1	95	111	--	--
186	CTRL1(15)	43	27	Note 1	Note 1	27	43	--	--
187	VCCA	--	--	--	--	--	--	--	--
188	CTRL2(15)	79	63	Note 1	Note 1	63	79	--	--
189	CTRL3(15)	115	99	Note 1	Note 1	99	115	--	--
190	CTRL1(7)	43	27	Note 1	Note 1	27	43	--	--
191	VTT	--	--	--	--	--	--	--	--
192	VCC	--	--	--	--	--	--	--	--
193	CTRL2(7)	79	63	Note 1	Note 1	63	79	--	--
194	CTRL3(7)	115	99	Note 1	Note 1	99	115	--	--
195	GND1	--	--	--	--	--	--	--	--
196	VCCA	--	--	--	--	--	--	--	--
197	VTT	--	--	--	--	--	--	--	--
198	VCC	--	--	--	--	--	--	--	--
199	GND1	--	--	--	--	--	--	--	--
200	DEST(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	DEST(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
202	DEST(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	DEST(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	DEST(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
205	DEST(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
206	DEST(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
207	DEST(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
208	DEST(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	DEST(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
210	DEST(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
211	DEST(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
212	DEST(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	DEST(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
214	DEST(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
215	VTT	--	--	--	--	--	--	--	--
216	VCC	--	--	--	--	--	--	--	--
217	DEST(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	ALUFLG(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
219	ALUFLG(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
220	ALUFLG(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
221	ALUFLG(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
222	ALUFLG(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	ALUFLG(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
224	ALUFLG(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
225	ALUFLG(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
226	STPMEM	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	ALULD	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	ACL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	DCL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	DBD(4)	--	--	Note 1	Note 1	--		Note 1	Note 1
231	DBD(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	DBD(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VTT	--	--	--	--	--	--	--	--
234	VCC	--	--	--	--	--	--	--	--
235	DBD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
236	DBD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
237	INIT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
238	SCPROT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
239	SBI(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
240	SBI(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
241	SBI(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
242	SBI(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
243	SBI(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
244	SBI(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MPY VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
245	SBI(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
246	SBI(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
247	SBI(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
248	SBI(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
249	SBI(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
250	GND1	--	--	--	--	--	--	--	--
251	VTT	--	--	--	--	--	--	--	--
252	VCC	--	--	--	--	--	--	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	GND	--	--	--	--	--	--	--	--
255	DDINT(0)	202	13	Note 1	Note 1	13	202	--	--
256	DDINT(1)	206	13	Note 1	Note 1	13	206	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on MPY-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP001 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V.

1. TPLH1 -- This parameter measures the time to detect a zero condition in the PRIEN logic circuit from the clock edge which loads the zero data word in the PED register. The PEZ output is used as a condition code in the sequencer. As such, it is edge triggered at the sequencer on the next rising edge of the clock. The maximum

acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures one important source in the OBP80 critical path (SRCMPY bus). The test vector for this parameter loads the CTRL1 register on the rising edge of the clock. This data passes through the control register selection mux, through the final source selection mux, and out the SRCMPY bus. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures a second data path using the CTRL1 register. The test vector for this parameter loads the CTRL1 register on the rising edge of the clock. This data passes directly to the CTRL1 outputs. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- This parameter measures a second important source in the OBP80 critical path to the SRCMPY bus. The test vector for this parameter utilizes the two different sources for the SRCMPY bus to measure the decoding delay through the final source selection mux. The SBS selection field toggles between two sources which have previously been defined The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures a third important source in the OBP80 critical path to the SRCMPY bus. The test vector for this parameter utilizes the SBI bus to directly pass data from the input receivers, through the final source selection mux, and out the SRCMPY bus. The SBS selection field has already been configured to pass the data through, so no decoding is included in this delay. The maximum acceptable value for this parameter is TBD nS.

6. TPLH6 -- This parameter measures the time required for the STPMEM signal to enable/disable the DDINT bus. The STPMEM signal is input to a programmable logic array, and is used as a qualifying enable for each of the DDINT signals. The maximum acceptable value for this parameter is TBD nS.

7. TPLH7 -- This parameter measures the time required for the source mux decode to change from source bus immediate field to control register 1. This measures the delay through the source mux selection path. The maximum acceptable value for this parameter is TBD nS.

Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

TABLE 5-2 AC Parametrics for MPY VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
38	TPLH1	199	PEZ	(CLK,CLKN); 25,23	TBD
37	TPLH2	15	SRCMPY(0)	(CLK,CLKN); 25,23	TBD
132	TPLH3	15	CTRL1(0)	(CLK,CLKN); 25,23	TBD
37	TPLH4	614	SRCMPY(0)	SBS=11-> SBS=10; 10	TBD
37	TPLH5	122	SRCMPY(0)	SBI(0); 39	TBD
4	TPLH6	218	DDINT(3)	STPMEM; 226	TBD
31	TPLH7	2114	SRCMPY(3)	SBS=06-> SBS=01:8,9,10	TBD
38	TPHL1	195	PEZ	(CLK,CLKN); 25,23	TBD
37	TPHL2	31	SRCMPY(0)	(CLK,CLKN); 25,23	TBD
132	TPHL3	31	CTRL1(0)	(CLK,CLKN); 25,23	TBD
37	TPHL4	618	SRCMPY(0)	SBS=10-> SBS=11; 10	TBD
37	TPHL5	138	SRCMPY(0)	SBI(0); 39	TBD

6. APPENDIX B -- MPY VLSI Burn-In Circuit

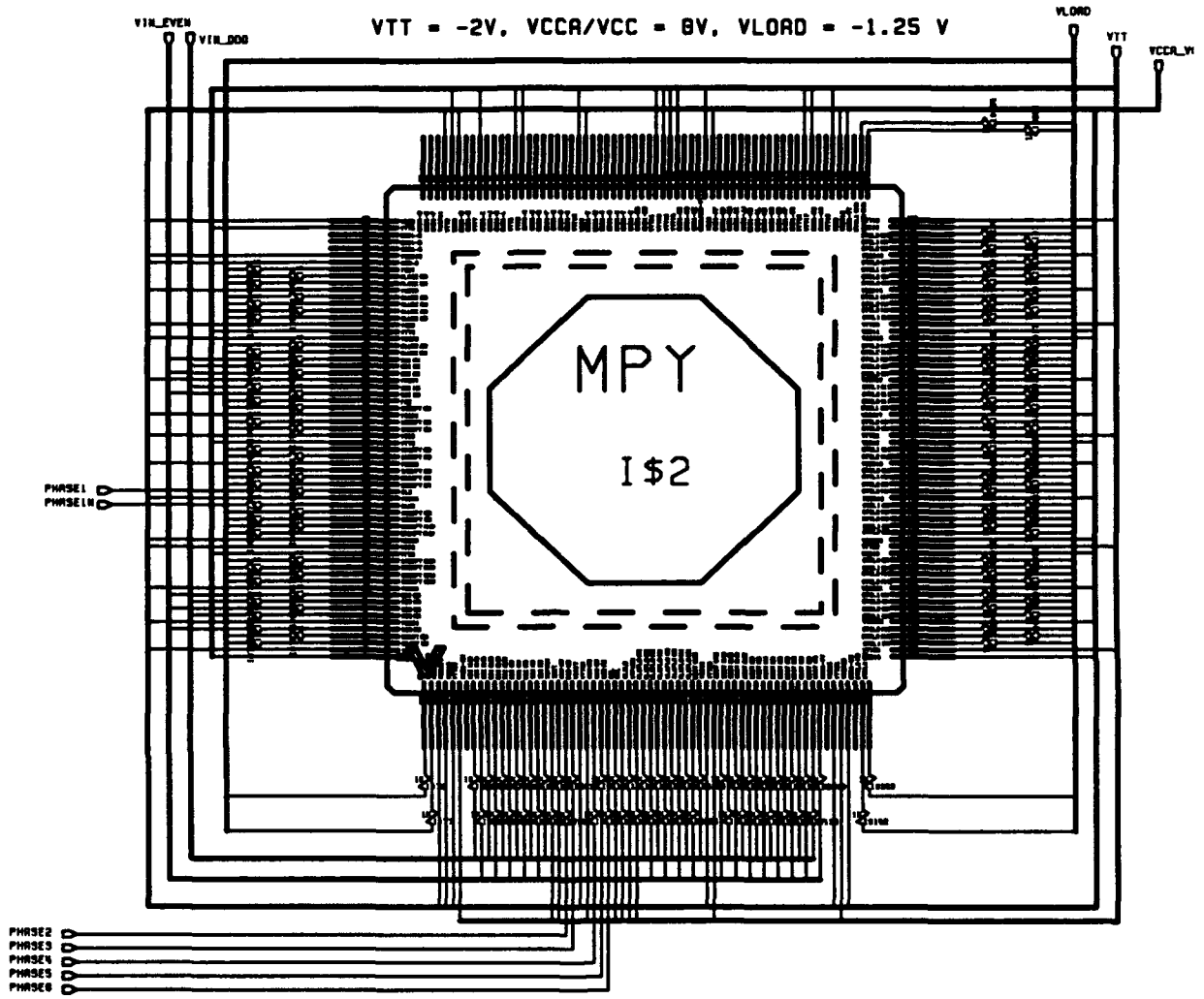

Figure 6-1 MPY VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- MPY VLSI Test Data Specification

All parametric data recorded on the MPY VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP002

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. Sheet 0 shall not be furnished to supplier.
2. The 'Dash 2' configuration refers to the initial wafer run for design characterization only.
3. Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.

PROGRAM AUTHORIZATION
Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION
Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Principal Design Engineer

Full Custom Dual Arithmetic Logic Unit for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP002	

SCALE	PAGE	SHEET
		0 of 40

Drawing Number: GOBP002

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	1/30/91	

											REV
				40	39	38	37	36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
											REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

Insertion Demonstrations of Digital Gallium Arsenide

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FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP002	
SCALE	PAGE	SHEET 1 of 40

Drawing Number: GOBP002

REVISIONS

REV	SH	DESCRIPTION	DATE	APPROVED

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP002	
SCALE	PAGE	SHEET 2 of 40

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom GALU VLSI; hereinafter referred to as GOBP002, GALU, or part.

1.2 Part Number - The GALU VLSI shall be identified by the part number GOBP002.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Case Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP002-MT1	Magnetic media functional description of GALU VLSI
GOBP002-MT2	Magnetic media graphical description of GALU VLSI
GOBP002-MT3	Magnetic media assembly drawing of GALU VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the GALU VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP002-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP002-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP002-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the GALU VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the GALU VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

The GALU VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification should be manufactured in a 1.2 micron, E/D GaAs MESFET process. Upon request, the vendor shall permit on site examination of process flow documentation for the purposes of determining process impact on device radiation hardness. Martin Marietta has performed the design of the GALU VLSI such that a device fabricated in the above mentioned process will exhibit the following characteristics:

3.2.6.1 Total Dose - Exposure to 3E4 rads (Si) total dose and exhibit no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec and not exhibit sustained latchup.

3.2.6.3 Single Particle Upset - Exposure to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec and not exhibit data loss from critical storage elements.

The above characteristics have been demonstrated on a device test vehicle representative of the technology. This specification does not require re-characterization explicitly for the GALU VLSI.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP002-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP002-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The GALU VLSI shall be packaged in a 344 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP002-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B. Since the dominant failure mechanism in this technology is electromigration, the burn in should attempt to equalize stress among the circuit paths. The static burn in circuit of Figure 6-1 should be used for all screening and qualification tests. To even out the stress, the following test procedure should be used at periods of 1/4 the total test duration:

a. The burn-in chamber should be brought to room temperature with the devices under bias, and the case temperature allowed to stabilize.

b. All bias should be removed from the device, and the case temperature allowed to stabilize.

c. After 30 minutes of dwell time at room temperature, return the bias to the device.

d. Ramp the burn-in chamber back to test temperature. The test shall be assumed to be in progress after the device case temperature has stabilized.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP002-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP002-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of GALU VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition B, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on GALU-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 11. The pattern drivers should be connected, and forcing pattern number 11. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.5 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 75. The patterns drivers should be connected, and forcing pattern number 75. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.5 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on GALU-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

3. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

4. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on GALU-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

3. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

4. VCD1P -- The Positive Current TerminatioonDiode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

5. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

6. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

In Table 5-1, the pins are listed sequentially from 1 to 344, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for GALU VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
1	VCC	--	--	--	--	--	--	--	--
2	VCCA	--	--	--	--	--	--	--	--
3	VCC	--	--	--	--	--	--	--	--
4	VTT	--	--	--	--	--	--	--	--
5	BRAN(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	BRAN(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
7	BRAN(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
8	BRAN(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
9	BRAN(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
10	BRAN(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
11	BRAN(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
12	BRAN(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
13	BRAN(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
14	BRAN(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
15	BRAN(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
16	BRAN(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
17	VCC	--	--	--	--	--	--	--	--
18	VTT	--	--	--	--	--	--	--	--
19	GND1	--	--	--	--	--	--	--	--
20	BRAN(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
21	BRAN(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
22	BRAN(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
23	BRAN(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
24	VCC	--	--	--	--	--	--	--	--
25	VCC	--	--	--	--	--	--	--	--
26	VCC	--	--	--	--	--	--	--	--
27	VCC	--	--	--	--	--	--	--	--
28	VTT	--	--	--	--	--	--	--	--
29	VTT	--	--	--	--	--	--	--	--
30	VTT	--	--	--	--	--	--	--	--
31	VTT	--	--	--	--	--	--	--	--
32	VCC	--	--	--	--	--	--	--	--
33	VTT	--	--	--	--	--	--	--	--
34	VCC	--	--	--	--	--	--	--	--
35	GND1	--	--	--	--	--	--	--	--
36	GND1	--	--	--	--	--	--	--	--
37	GND1	--	--	--	--	--	--	--	--
38	GND1	--	--	--	--	--	--	--	--
39	GND1	--	--	--	--	--	--	--	--
40	GND1	--	--	--	--	--	--	--	--
41	LYE	--	--	Note 1	Note 1	--	--	Note 1	Note 1
42	DBS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
43	DBS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
44	DCIN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
45	DCS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
46	DCS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
47	VCC	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	DSS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
50	DSS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
51	DSS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
52	DIS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
53	DIS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
54	DIS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
55	DIF(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
56	DIF(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
57	DIF(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
58	DID(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
59	DID(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
60	DID(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
61	VCC	--	--	--	--	--	--	--	--
62	VTT	--	--	--	--	--	--	--	--
63	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
64	GND1	--	--	--	--	--	--	--	--
65	GND1	--	--	--	--	--	--	--	--
66	GND1	--	--	--	--	--	--	--	--
67	DID(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
68	VTT	--	--	--	--	--	--	--	--
69	VCCA	--	--	--	--	--	--	--	--
70	VTT	--	--	--	--	--	--	--	--
71	DBD(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
72	DBD(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
73	DBD(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
74	VCCA	--	--	--	--	--	--	--	--
75	DBD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
76	VCC	--	--	--	--	--	--	--	--
77	VTT	--	--	--	--	--	--	--	--
78	DBD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
79	DAB(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
80	DAB(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
81	VCCA	--	--	--	--	--	--	--	--
82	DAB(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
83	DAB(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
84	DAB(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
85	DAB(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
86	VCCA	--	--	--	--	--	--	--	--
87	VCC	--	--	--	--	--	--	--	--
88	VCC	--	--	--	--	--	--	--	--
89	DAA(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
90	VCC	--	--	--	--	--	--	--	--
91	VTT	--	--	--	--	--	--	--	--
92	DAA(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
93	VCC	--	--	--	--	--	--	--	--
94	VTT	--	--	--	--	--	--	--	--
95	VTT	--	--	--	--	--	--	--	--
96	VCC	--	--	--	--	--	--	--	--
97	DAA(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
98	VCCA	--	--	--	--	--	--	--	--
99	DAA(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
100	DAA(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
101	DAA(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
102	SBS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
103	VCCA	--	--	--	--	--	--	--	--
104	VCC	--	--	--	--	--	--	--	--
105	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
106	SBS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
107	SBS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
108	SBS(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
109	SBS(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
110	VCCA	--	--	--	--	--	--	--	--
111	DTST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
112	TSTECC	--	--	Note 1	Note 1	--	--	Note 1	Note 1
113	ATST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
114	STALL(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
115	VCCA	--	--	--	--	--	--	--	--
116	STALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
117	STALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
118	VCC	--	--	--	--	--	--	--	--
119	VTT	--	--	--	--	--	--	--	--
120	STALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
121	STALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
122	VCCA	--	--	--	--	--	--	--	--
123	STALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
124	AAAX(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
125	AAAX(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
126	AAAX(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
127	VCCA	--	--	--	--	--	--	--	--
128	AAAX(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
129	AAAX(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
130	AAAX(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
131	AABX(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
132	VCC	--	--	--	--	--	--	--	--
133	VTT	--	--	--	--	--	--	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	AABX(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
136	AABX(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
137	AABX(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
138	AABX(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
139	VCCA	--	--	--	--	--	--	--	--
140	AABX(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
141	VCC	--	--	--	--	--	--	--	--
142	VTT	--	--	--	--	--	--	--	--
143	VTT	--	--	--	--	--	--	--	--
144	VCC	--	--	--	--	--	--	--	--
145	INITF	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
146	VCC	--	--	--	--	--	--	--	--
147	VTT	--	--	--	--	--	--	--	--
148	SBI(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
149	VCC	--	--	--	--	--	--	--	--
150	VCC	--	--	--	--	--	--	--	--
151	VCCA	--	--	--	--	--	--	--	--
152	SBI(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
153	SBI(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
154	SBI(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
155	SBI(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
156	VCCA	--	--	--	--	--	--	--	--
157	SBI(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
158	SBI(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
159	SBI(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
160	VCC	--	--	--	--	--	--	--	--
161	VTT	--	--	--	--	--	--	--	--
162	SBI(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
163	VCCA	--	--	--	--	--	--	--	--
164	SBI(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
165	SBI(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
166	SBI(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
167	SBI(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
168	VCCA	--	--	--	--	--	--	--	--
169	SBI(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
170	SBI(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
171	SBI(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
172	GND1	--	--	--	--	--	--	--	--
173	GND1	--	--	--	--	--	--	--	--
174	VCCA	--	--	--	--	--	--	--	--
175	VCC	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--
177	AID(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
178	AID(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
179	AIF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
180	AIS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
181	AIS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
182	AIS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
183	ACI	--	--	Note 1	Note 1	--	--	Note 1	Note 1
184	ASS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
185	ASS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
186	ACIN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
187	ABD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
188	ABD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
189	VCC	--	--	--	--	--	--	--	--
190	VTT	--	--	--	--	--	--	--	--
191	SDM0(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
192	SDM0(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
193	SDM0(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
194	SDM0(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
195	SDM0(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
196	SDM0(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
197	SDM0(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
198	SDM0(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
199	SDM0(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
200	SDM0(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	SDM0(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
202	SDM0(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	SDM0(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	VCC	--	--	--	--	--	--	--	--
205	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
206	SDM0(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
207	SDM0(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
208	SDM0(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	VCC	--	--	--	--	--	--	--	--
210	VTT	--	--	--	--	--	--	--	--
211	VCC	--	--	--	--	--	--	--	--
212	SDM1(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	SDM1(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
214	SDM1(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
215	SDM1(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
216	VCC	--	--	--	--	--	--	--	--
217	DM1CB	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	VTT	--	--	--	--	--	--	--	--
219	VCC	--	--	--	--	--	--	--	--
220	VTT	--	--	--	--	--	--	--	--
221	SDM1(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
222	SDM1(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	SDM1(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
224	SDM1(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
225	SDM1(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
226	SDM1(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	SDM1(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	SDM1(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	SDM1(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	SDM1(13)	--	--	Note 1	Note 1	--		Note 1	Note 1
231	SDM1(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	SDM1(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VCC	--	--	--	--	--	--	--	--
234	VTT	--	--	--	--	--	--	--	--
235	VCCA	--	--	--	--	--	--	--	--
236	GND1	--	--	--	--	--	--	--	--
237	ADDR(0)	85	13	Note 1	Note 1	13	85	--	--
238	ADDR(1)	89	17	Note 1	Note 1	17	89	--	--
239	ADDR(2)	93	21	Note 1	Note 1	21	93	--	--
240	ADDR(3)	97	25	Note 1	Note 1	25	97	--	--
241	VCCA	--	--	--	--	--	--	--	--
242	ADDR(4)	101	29	Note 1	Note 1	29	101	--	--
243	ADDR(5)	105	33	Note 1	Note 1	33	105	--	--
244	ADDR(6)	109	37	Note 1	Note 1	37	109	--	--
245	ADDR(7)	113	41	Note 1	Note 1	41	113	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
246	VCCA	--	--	--	--	--	--	--	--
247	ADDR(8)	117	45	Note 1	Note 1	45	117	--	--
248	VCC	--	--	--	--	--	--	--	--
249	VTT	--	--	--	--	--	--	--	--
250	ADDR(9)	121	49	Note 1	Note 1	49	121	--	--
251	ADDR(10)	125	53	Note 1	Note 1	53	125	--	--
252	ADDR(11)	129	57	Note 1	Note 1	57	129	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	ADDR(12)	133	61	--	--	61	133	--	--
255	ADDR(13)	137	65	Note 1	Note 1	65	137	--	--
256	ADDR(14)	141	69	Note 1	Note 1	69	141	--	--
257	ADDR(15)	145	73	Note 1	Note 1	73	145	--	--
258	VCCA	--	--	--	--	--	--	--	--
259	ACC(0)	345	341	Note 1	Note 1	341	345	--	--
260	ACC(1)	345	341	Note 1	Note 1	341	345	--	--
261	ACC(2)	357	353	Note 1	Note 1	353	357	--	--
262	VCC	--	--	--	--	--	--	--	--
263	VTT	--	--	--	--	--	--	--	--
264	ACC(3)	357	353	Note 1	Note 1	353	357	--	--
265	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
266	SMPY(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
267	SMPY(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
268	SMPY(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
269	SMPY(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
270	VCCA	--	--	--	--	--	--	--	--
271	SMPY(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
272	SMPY(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
273	SMPY(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
274	SMPY(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
275	VCCA	--	--	--	--	--	--	--	--
276	VCC	--	--	--	--	--	--	--	--
277	VTT	--	--	--	--	--	--	--	--
278	SMPY(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
279	SMPY(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
280	SMPY(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
281	SMPY(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
282	VCCA	--	--	--	--	--	--	--	--
283	SMPY(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
284	SMPY(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
285	SMPY(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
286	SMPY(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
287	VCCA	--	--	--	--	--	--	--	--
288	CLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
289	CLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
290	VCC	--	--	--	--	--	--	--	--
291	SEAL RING VTT	--	--	--	--	--	--	--	--
292	GND1	--	--	--	--	--	--	--	--
293	DCC(0)	321	317	Note 1	Note 1	317	321	--	--
294	VCCA	--	--	--	--	--	--	--	--
295	DCC(1)	321	317	Note 1	Note 1	317	321	--	--
296	DCC(2)	333	329	Note 1	Note 1	329	333	--	--
297	DCC(3)	333	329	Note 1	Note 1	329	333	--	--
298	DEST1(15)	145	73	Note 1	Note 1	73	145	--	--
299	VCCA	--	--	--	--	--	--	--	--
300	DEST0(15)	145	73	Note 1	Note 1	73	145	--	--
301	DEST1(14)	141	69	Note 1	Note 1	69	141	--	--
302	DEST0(14)	141	69	Note 1	Note 1	69	141	--	--
303	DEST1(13)	137	65	Note 1	Note 1	65	137	--	--
304	VCC	--	--	--	--	--	--	--	--
305	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
306	VCCA	--	--	--	--	--	--	--	--
307	DEST0(13)	137	65	Note 1	Note 1	57	129	--	--
308	DEST1(12)	133	61	Note 1	Note 1	53	125	--	--
309	DEST0(12)	133	61	Note 1	Note 1	53	125	--	--
310	DEST1(11)	129	57	Note 1	Note 1	49	121	--	--
311	VCCA	--	--	--	--	--	--	--	--
312	DEST0(11)	129	57	Note 1	Note 1	57	129	--	--
313	DEST1(10)	125	53	Note 1	Note 1	53	125	--	--
314	DEST0(10)	125	53	Note 1	Note 1	53	125	--	--
315	DEST1(9)	121	49	Note 1	Note 1	49	121	--	--
316	VCCA	--	--	--	--	--	--	--	--
317	DEST0(9)	121	49	Note 1	Note 1	49	121	--	--
318	VCC	--	--	--	--	--	--	--	--
319	VTT	--	--	--	--	--	--	--	--
320	DEST1(8)	117	45	Note 1	Note 1	45	117	--	--
321	DEST0(8)	117	45	Note 1	Note 1	45	117	--	--
322	DEST1(7)	113	41	Note 1	Note 1	41	113	--	--
323	VCCA	--	--	--	--	--	--	--	--
324	DEST0(7)	113	41	Note 1	Note 1	41	113	--	--
325	DEST1(6)	109	37	Note 1	Note 1	37	109	--	--

TABLE 5-1 DC Parametrics for GALU VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
326	DEST0(6)	109	37	Note 1	Note 1	37	109	--	--
327	DEST1(5)	105	33	Note 1	Note 1	33	105	--	--
328	VCCA	--	--	--	--	--	--	--	--
329	DEST0(5)	105	33	Note 1	Note 1	33	105	--	--
330	DEST1(4)	101	29	Note 1	Note 1	29	101	--	--
331	DEST0(4)	101	29	Note 1	Note 1	29	101	--	--
332	VCC	--	--	--	--	--	--	--	--
333	VTT	--	--	--	--	--	--	--	--
334	DEST1(3)	97	25	Note 1	Note 1	25	97	--	--
335	VCCA	--	--	--	--	--	--	--	--
336	DEST0(3)	97	25	Note 1	Note 1	25	97	--	--
337	DEST1(2)	93	21	Note 1	Note 1	21	93	--	--
338	DEST0(2)	93	21	Note 1	Note 1	21	93	--	--
339	DEST1(1)	89	17	Note 1	Note 1	17	89	--	--
340	VCCA	--	--	--	--	--	--	--	--
341	DEST0(1)	89	17	Note 1	Note 1	17	89	--	--
342	DEST1(0)	85	13	Note 1	Note 1	13	85	--	--
343	DEST0(0)	85	13	Note 1	Note 1	13	85	--	--
344	VCC	--	--	--	--	--	--	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on GALU-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP002 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V. Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

1. TPLH1 -- This parameter measures the time to pass data directly from the BRAN bus to the DEST0 and DEST1 busses. The test pattern used for this measurement has the DBS (Destination Bus Source select) field = 2. This bypasses the ALU, passing instead through the DESTMUX to the output pins. Consequently, this measurement is 'flow through', and is not referenced to the clock. The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures one important processing delay in the OBP80 critical path (Data in through SMPY bus to DATA ALU to DESTMUX to DESTn bus). The test vector for this parameter performs an 'ADD' instruction in the data ALU. This data passes through the DSRCMUX, DALU, and out through the DESTMUX. Carry In is assumed to be setup ahead of time. This test adds 1 to 7FFF (FFFF for TPHL) when the previous data has been zero. This measurement is also 'flow through', and is not referenced to the clock. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures a similar data path to TPHL2. This time the processing delay is 'Data in through SMPY bus to ADDR ALU to ADDR bus'. This data passes through the ASRCMUX, AALU, and directly out the ADDR bus. The data from THLH3 applies to this measurement. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- The data for this measurement is identical to TPLH2. However, this measurement is made on the 'ZERO' condition code. This measurement is critical to the OBP80 since the condition codes are latched in the MPY VLSI device. The data path is 'Data in through SMPY bus to DATA ALU to zero detect to DCC(0). The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures a third OBP80 critical path. The control bits select a 'new' register file operand as the data source. This forces a RAM access from the register file. The initial state of the ALU was producing a 0001, and is forced to 0000 by adding the carry in to FFFF from the register file. The data path for this instruction is 'DAA to Register file out to Data ALU to zero detect to DCC(0)'. The maximum acceptable value for this parameter is TBD nS.

TABLE 5-2 AC Parametrics for GALU VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
300	TPLH1	365	DEST0(15)	BRAN(15); 23	TBD
300	TPLH2	385	DEST0(15)	SMPY(15); 266	TBD
257	TPLH3	413	ADDR(15)	SMPY(15); 266	TBD
293	TPLH4	393	DCC(0)	SMPY(0); 286	TBD
293	TPLH5	457	DCC(0)	DAA(0); 101	TBD
300	TPHL1	373	DEST0(15)	BRAN(15); 23	TBD
300	TPHL2	393	DEST0(15)	SMPY(15); 266	TBD
257	TPHL3	421	ADDR(15)	SMPY(15); 266	TBD
293	TPHL4	397	DCC(0)	SMPY(0); 286	TBD
293	TPHL5	465	DCC(0)	DAA(0); 101	TBD

6. APPENDIX B -- GALU VLSI Burn-In Circuit

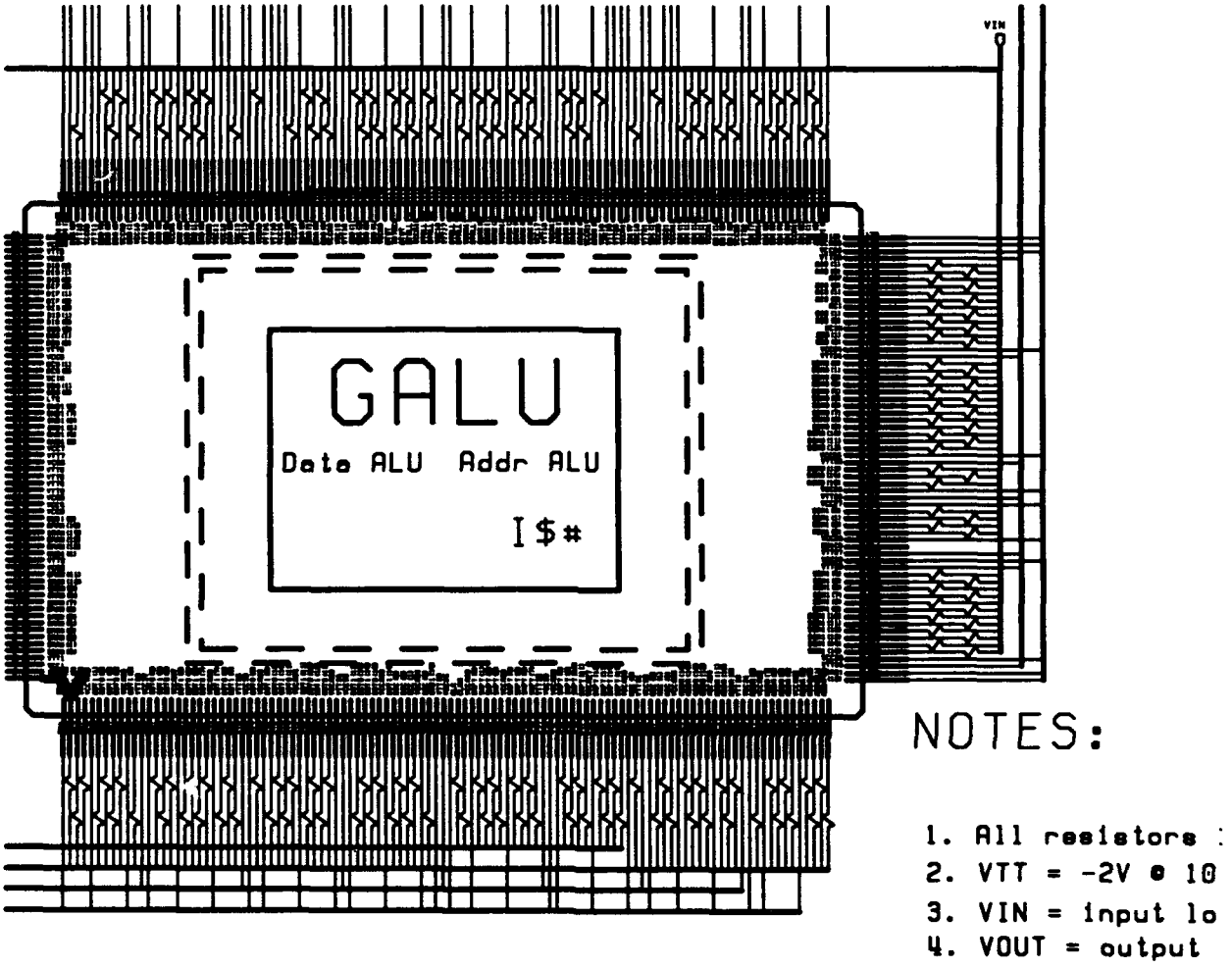

Figure 6-1 GALU VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- GALU VLSI Test Data Specification

All parametric data recorded on the GALU VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP003

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. Sheet 0 shall not be furnished to supplier.
2. The 'Dash 2' configuration refers to the initial wafer run for design characterization only.
3. Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.

PROGRAM AUTHORIZATION
Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION
Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Principal Design Engineer

Full Custom Intelligent Pipeline Register for GaAs OBP

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP003	
SCALE	PAGE	SHEET 0 of 42

Drawing Number: GOBP003

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	3/7/91	
	Revision A	**5/18/91**	

						A	A				REV
		42	41	40	39	38	37	36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
					A	A	A				REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

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Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

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Full Custom Intelligent Pipeline Register for GaAs OBP

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP003	A
SCALE	PAGE	SHEET 1 of 42

Drawing Number: GOBP003

REVISIONS

REV	SH	DESCRIPTION	DATE	APPROVED
A	15 16 17	Added DC parametric test conditions for ECL inputs.		
A	15	Corrected error in specified pattern number for AC tests.		

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP003	A
SCALE	PAGE	SHEET 2 of 42

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom IPR VLSI; hereinafter referred to as GOBP003, IPR, or part.

1.2 Part Number - The IPR VLSI shall be identified by the part number GOBP003.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Case Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP003-MT1	Magnetic media functional description of IPR VLSI
GOBP003-MT2	Magnetic media graphical description of IPR VLSI
GOBP003-MT3	Magnetic media assembly drawing of IPR VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the IPR VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP003-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP003-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP003-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the IPR VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the IPR VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

The IPR VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification should be manufactured in a 1.2 micron, E/D GaAs MESFET process. Upon request, the vendor shall permit on site examination of process flow documentation for the purposes of determining process impact on device radiation hardness. Martin Marietta has performed the design of the IPR VLSI such that a device fabricated in the above mentioned process will exhibit the following characteristics:

3.2.6.1 Total Dose - Exposure to 3E4 rads (Si) total dose and exhibit no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec and not exhibit sustained latchup.

3.2.6.3 Single Particle Upset - Exposure to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec and not exhibit data loss from critical storage elements.

The above characteristics have been demonstrated on a device test vehicle representative of the technology. This specification does not require re-characterization explicitly for the IPR VLSI.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP003-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP003-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The IPR VLSI shall be packaged in a 344 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP003-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B. Since the dominant failure mechanism in this technology is electromigration, the burn in should attempt to equalize stress among the circuit paths. The static burn in circuit of Figure 6-1 should be used for all screening and qualification tests. To even out the stress, the following test procedure should be used at periods of 1/4 the total test duration:

a. The burn-in chamber should be brought to room temperature with the devices under bias, and the case temperature allowed to stabilize.

b. All bias should be removed from the device, and the case temperature allowed to stabilize.

c. After 30 minutes of dwell time at room temperature, return the bias to the device.

d. Ramp the burn-in chamber back to test temperature. The test shall be assumed to be in progress after the device case temperature has stabilized.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP003-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP003-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of IPR VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition B, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on IPR-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 11. The pattern drivers should be connected, and forcing pattern number 11. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.5 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 75. The patterns drivers should be connected, and forcing pattern number 75. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.5 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on IPR-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The GaAs Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIH ECL 100K -- The ECL Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.2 V

3. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

4. VIL ECL 100K -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

5. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

6. IIH ECL 100K -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

7. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

8. IIL ECL 100K -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

9. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

10. VCD1N ECL 100K -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

    IOL = -3 mA, VTT = VCCA = VCC = 0 V.

11. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

12. VCD1P ECL 100K -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on IPR-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

3. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

4. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

5. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

6. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

In Table 5-1, the pins are listed sequentially from 1 to 344, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for IPR VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
1	VREF (-1.3V)	--	--	--	--	--	--	--	--
2	VCCA	--	--	--	--	--	--	--	--
3	VCC	--	--	--	--	--	--	--	--
4	VTT	--	--	--	--	--	--	--	--
5	WCS(47) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	WCS(46) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
7	WCS(45) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
8	WCS(44) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
9	WCS(43) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
10	WCS(42) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
11	WCS(41) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
12	WCS(40) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
13	WCS(39) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
14	WCS(38) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
15	WCS(37) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
16	WCS(36) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
17	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
18	VTT	--	--	--	--	--	--	--	--
19	WCS(35) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
20	WCS(34) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
21	WCS(33) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
22	WCS(32) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
23	WCS(31) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
24	WCS(30) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
25	WCS(29) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
26	WCS(28) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
27	WCS(27) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
28	WCS(26) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
29	WCS(25) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
30	WCS(24) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
31	WCS(23) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
32	VCC	--	--	--	--	--	--	--	--
33	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
34	WCS(22) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
35	WCS(21) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
36	WCS(20) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
37	WCS(19) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
38	WCS(18) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
39	WCS(17) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
40	WCS(16) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
41	WCS(15) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
42	WCS(14) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
43	WCS(13) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
44	WCS(12) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
45	WCS(11) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
46	VREF (-1.3V)	--	--	--	--	--	--	--	--
47	VCC	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	WCS(10) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
50	WCS(9) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
51	WCS(8) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
52	WCS(7) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
53	WCS(6) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
54	WCS(5) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
55	WCS(4) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
56	WCS(3) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
57	WCS(2) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
58	WCS(1) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
59	WCS(0) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
60	SDIN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
61	VCC	--	--	--	--	--	--	--	--
62	VTT	--	--	--	--	--	--	--	--
63	VCCA	--	--	--	--	--	--	--	--
64	PS1(0)	16	12	Note 1	Note 1	12	16	--	--
65	PS1(1)	20	16	Note 1	Note 1	16	20	--	--
66	PS1(2)	24	20	Note 1	Note 1	20	24	--	--
67	PS1(3)	28	24	Note 1	Note 1	24	28	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
68	PS1(4)	32	28	Note 1	Note 1	28	32	--	--
69	VCCA	--	--	--	--	--	--	--	--
70	PS1(5)	36	32	Note 1	Note 1	32	36	--	--
71	PS1(6)	40	36	Note 1	Note 1	36	40	--	--
72	PS1(7)	44	40	Note 1	Note 1	40	44	--	--
73	PS1(8)	48	44	Note 1	Note 1	44	48	--	--
74	VCCA	--	--	--	--	--	--	--	--
75	PS1(9)	52	48	Note 1	Note 1	48	52	--	--
76	VCC	--	--	--	--	--	--	--	--
77	VTT	--	--	--	--	--	--	--	--
78	PS1(10)	56	52	Note 1	Note 1	52	56	--	--
79	PS1(11)	60	56	Note 1	Note 1	56	60	--	--
80	PS1(12)	64	60	Note 1	Note 1	60	64	--	--
81	VCCA	--	--	--	--	--	--	--	--
82	PS1(13)	68	64	Note 1	Note 1	64	68	--	--
83	PS1(14)	72	68	Note 1	Note 1	68	72	--	--
84	PS1(15)	76	72	Note 1	Note 1	72	76	--	--
85	PERR(0)	3196	3193	Note 1	Note 1	3193	3196	--	--
86	VCCA	--	--	--	--	--	--	--	--
87	WCS(48) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
88	WCS(49) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
89	WCS(50) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
90	VCC	--	--	--	--	--	--	--	--
91	VTT	--	--	--	--	--	--	--	--
92	WCS(51) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
93	VCCA	--	--	--	--	--	--	--	--
94	WCS(52) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
95	WCS(53) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
96	WCS(54) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
97	WCS(55) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
98	VCCA	--	--	--	--	--	--	--	--
99	VREF (-1.3V)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
100	WCS(56) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
101	WCS(57) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
102	WCS(58) ECL 100K	--	-	Note 1	Note 1	--	--	Note 1	Note 1
103	VCCA	--	--	--	--	--	--	--	--
104	VCC	--	--	--	--	--	--	--	--
105	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
106	WCS(59) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
107	WCS(60) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
108	WCS(61) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
109	WCS(62) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
110	VCCA	--	--	--	--	--	--	--	--
111	WCS(63) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
112	GO	--	--	Note 1	Note 1	--	--	Note 1	Note 1
113	STALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
114	STALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
115	VCCA	--	--	--	--	--	--	--	--
116	STALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
117	VTT	--	--	--	--	--	--	--	--
118	VCC	--	--	--	--	--	--	--	--
119	VTT	--	--	--	--	--	--	--	--
120	CLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
121	CLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
122	VCCA	--	--	--	--	--	--	--	--
123	STALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
124	STALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
125	INITF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
126	PEVEN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
127	VCCA	--	--	--	--	--	--	--	--
128	TEST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
129	PIPESEL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
130	SSEL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
131	SSEL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
132	VCC	--	--	--	--	--	--	--	--
133	VTT	--	--	--	--	--	--	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	PS2(63)	268	264	Note 1	Note 1	264	268	--	--
136	PS2(62)	264	260	Note 1	Note 1	260	264	--	--
137	PS2(61)	260	256	Note 1	Note 1	256	260	--	--
138	PS2(60)	256	252	Note 1	Note 1	252	256	--	--
139	VCCA	--	--	--	--	--	--	--	--
140	PS2(59)	252	248	Note 1	Note 1	248	252	--	--
141	PS2(58)	248	244	Note 1	Note 1	244	248	--	--
142	PS2(57)	244	240	Note 1	Note 1	240	244	--	--
143	PS2(56)	240	236	Note 1	Note 1	236	240	--	--
144	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
145	PS2(79)	332	328	Note 1	Note 1	328	332	--	--
146	VCC	--	--	--	--	--	--	--	--
147	VTT	--	--	--	--	--	--	--	--
148	PS2(78)	328	324	Note 1	Note 1	324	328	--	--
149	PS2(77)	324	320	Note 1	Note 1	320	324	--	--
150	PS2(76)	320	316	Note 1	Note 1	316	320	--	--
151	VCCA	--	--	--	--	--	--	--	--
152	PS2(75)	316	312	Note 1	Note 1	312	316	--	--
153	PS2(74)	312	308	Note 1	Note 1	308	312	--	--
154	PS2(73)	308	304	Note 1	Note 1	304	308	--	--
155	PS2(72)	304	300	Note 1	Note 1	300	304	--	--
156	VCCA	--	--	--	--	--	--	--	--
157	PS2(71)	300	296	Note 1	Note 1	296	300	--	--
158	PS2(70)	296	292	Note 1	Note 1	292	296	--	--
159	PS2(69)	292	288	Note 1	Note 1	288	292	--	--
160	VCC	--	--	--	--	--	--	--	--
161	VTT	--	--	--	--	--	--	--	--
162	PS2(68)	288	284	Note 1	Note 1	284	288	--	--
163	VCCA	--	--	--	--	--	--	--	--
164	PS4(68)	288	284	Note 1	Note 1	284	288	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
165	PS2(67)	284	280	Note 1	Note 1	280	284	--	--
166	PS4(67)	284	280	Note 1	Note 1	280	284	--	--
167	PS2(66)	280	276	Note 1	Note 1	276	280	--	--
168	VCCA	--	--	--	--	--	--	--	--
169	PS4(66)	280	276	Note 1	Note 1	276	280	--	--
170	PS2(65)	276	272	Note 1	Note 1	272	276	--	--
171	PS4(65)	276	272	Note 1	Note 1	272	276	--	--
172	PS2(64)	272	268	Note 1	Note 1	268	272	--	--
173	PS4(64)	272	268	Note 1	Note 1	268	272	--	--
174	VCCA	--	--	--	--	--	--	--	--
175	VCC	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--
177	WCS(64) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
178	WCS(65) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
179	WCS(66) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
180	WCS(67) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
181	WCS(68) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
182	WCS(69) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
183	WCS(70) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
184	WCS(71) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
185	WCS(72) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
186	WCS(73) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
187	WCS(74) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
188	WCS(75) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
189	VCC	--	--	--	--	--	--	--	--
190	VTT	--	--	--	--	--	--	--	--
191	VREF (-1.3V)	--	--	--	--	--	--	--	--
192	WCS(76) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
193	WCS(77) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
194	WCS(78) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
195	WCS(79) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
196	WCS(80) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
197	WCS(81) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
198	WCS(82) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
199	WCS(83) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
200	WCS(84) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	WCS(85) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
202	WCS(86) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	WCS(87) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	VCC	--	--	--	--	--	--	--	--
205	VTT	--	--	--	--	--	--	--	--
206	WCS(88) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
207	WCS(89) ECL 100K	--	-	Note 1	Note 1	--	--	Note 1	Note 1
208	WCS(90) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	WCS(91) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
210	WCS(92) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
211	WCS(93) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
212	WCS(94) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	WCS(95) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
214	WCS(96) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
215	WCS(97) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
216	WCS(98) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
217	WCS(99) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	PARDIS	--	--	Note 1	Note 1	--	--	Note 1	Note 1
219	VCC	--	--	--	--	--	--	--	--
220	VTT	--	--	--	--	--	--	--	--
221	WCS(100) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
222	WCS(101) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	WCS(102) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
224	WCS(103) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
225	WCS(104) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
226	WCS(105) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	WCS(106) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	WCS(107) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	WCS(108) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	WCS(109) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
231	WCS(110) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	WCS(111) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VCC	--	--	--	--	--	--	--	--
234	VTT	--	--	--	--	--	--	--	--
235	VCCA	--	--	--	--	--	--	--	--
236	VREF (-1.3V)	--	--	--	--	--	--	--	--
237	GND1	--	--	--	--	--	--	--	--
238	PS2(80)	336	332	Note 1	Note 1	332	336	--	--
239	PS2(81)	340	336	Note 1	Note 1	336	340	--	--
240	PS2(82)	344	340	Note 1	Note 1	340	344	--	--
241	VCCA	--	--	--	--	--	--	--	--
242	PS2(83)	348	344	Note 1	Note 1	344	348	--	--
243	PS2(84)	352	348	Note 1	Note 1	348	352	--	--
244	PS2(85)	356	352	Note 1	Note 1	352	356	--	--
245	PS2(86)	360	356	Note 1	Note 1	356	360	--	--
246	VCCA	--	--	--	--	--	--	--	--
247	PS2(87)	364	360	Note 1	Note 1	360	364	--	--
248	VCC	--	--	--	--	--	--	--	--
249	VTT	--	--	--	--	--	--	--	--
250	PS2(96)	400	396	Note 1	Note 1	396	400	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
251	PS2(97)	404	400	Note 1	Note 1	400	404	--	--
252	PS2(98)	408	404	Note 1	Note 1	404	408	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	PS2(99)	412	408	Note 1	Note 1	408	412	--	--
255	PS2(100)	416	412	Note 1	Note 1	412	416	--	--
256	PS2(101)	420	416	Note 1	Note 1	416	420	--	--
257	PERR(2)	3196	3193	Note 1	Note 1	3193	3196	--	--
258	VCCA	--	--	--	--	--	--	--	--
259	PS3(103)	428	424	Note 1	Note 1	424	428	--	--
260	PS3(104)	432	428	Note 1	Note 1	428	432	--	--
261	PS3(105)	436	432	Note 1	Note 1	432	436	--	--
262	VCC	--	--	--	--	--	--	--	--
263	VTT	--	--	--	--	--	--	--	--
264	PS3(106)	440	436	Note 1	Note 1	436	440	--	--
265	VCCA	--	--	--	--	--	--	--	--
266	PS3(107)	444	440	Note 1	Note 1	440	444	--	--
267	PS3(108)	448	444	Note 1	Note 1	444	448	--	--
268	PS3(109)	452	448	Note 1	Note 1	448	452	--	--
269	PS3(110)	456	452	Note 1	Note 1	452	456	--	--
270	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
271	PS3(111)	460	456	Note 1	Note 1	456	460	--	--
272	PS2(88)	368	364	Note 1	Note 1	364	368	--	--
273	PS2(89)	372	368	Note 1	Note 1	368	372	--	--
274	PS2(90)	376	372	Note 1	Note 1	372	376	--	--
275	VCCA	--	--	--	--	--	--	--	--
276	VCC	--	--	--	--	--	--	--	--
277	VTT	--	--	--	--	--	--	--	--
278	PS2(91)	380	376	Note 1	Note 1	376	380	--	--
279	PS2(92)	384	380	Note 1	Note 1	380	384	--	--
280	PS2(93)	388	384	Note 1	Note 1	384	388	--	--
281	PS2(94)	392	388	Note 1	Note 1	388	392	--	--
282	VCCA	--	--	--	--	--	--	--	--
283	PS2(95)	396	392	Note 1	Note 1	392	396	--	--
284	SDOUT	1816	1812	Note 1	Note 1	1812	1816	--	--
285	PS2(55)	236	232	Note 1	Note 1	232	236	--	--
286	PS2(54)	232	228	Note 1	Note 1	228	232	--	--
287	VCCA	--	--	--	--	--	--	--	--
288	PS2(53)	228	224	Note 1	Note 1	224	228	--	--
289	PS2(52)	224	220	Note 1	Note 1	220	224	--	--
290	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
291	SEAL RING VTT	--	--	--	--	--	--	--	--
292	PS2(51)	220	216	Note 1	Note 1	216	220	--	--
293	PS2(50)	216	212	Note 1	Note 1	212	216	--	--
294	VCCA	--	--	--	--	--	--	--	--
295	PS2(49)	212	208	Note 1	Note 1	208	212	--	--
296	PS2(48)	208	204	Note 1	Note 1	204	208	--	--
297	BITFAIL	5484	5485	Note 1	Note 1	5485	5484	--	--
298	PS2(31)	140	136	Note 1	Note 1	136	140	--	--
299	VCCA	--	--	--	--	--	--	--	--
300	PERR(1)	3196	3193	Note 1	Note 1	3193	3196	--	--
301	PS1(29)	132	128	Note 1	Note 1	128	132	--	--
302	PS1(28)	128	124	Note 1	Note 1	124	128	--	--
303	PS1(27)	124	120	Note 1	Note 1	120	124	--	--
304	VCC	--	--	--	--	--	--	--	--
305	VTT	--	--	--	--	--	--	--	--
306	VCCA	--	--	--	--	--	--	--	--
307	PS1(26)	120	116	Note 1	Note 1	116	120	--	--
308	PS1(25)	116	112	Note 1	Note 1	112	116	--	--
309	PS1(24)	112	108	Note 1	Note 1	108	112	--	--
310	PS2(47)	204	200	Note 1	Note 1	200	204	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
311	VCCA	--	--	--	--	--	--	--	--
312	PS2(46)	200	196	Note 1	Note 1	196	200	--	--
313	PS2(45)	196	192	Note 1	Note 1	192	196	--	--
314	PS2(44)	192	188	Note 1	Note 1	188	192	--	--
315	PS2(43)	188	184	Note 1	Note 1	184	188	--	--
316	VCCA	--	--	--	--	--	--	--	--
317	PS2(42)	184	180	Note 1	Note 1	180	184	--	--
318	VCC	--	--	--	--	--	--	--	--
319	VTT	--	--	--	--	--	--	--	--
320	PS2(41)	180	176	Note 1	Note 1	176	180	--	--
321	PS2(40)	176	172	Note 1	Note 1	172	176	--	--
322	PS2(39)	172	168	Note 1	Note 1	168	172	--	--
323	VCCA	--	--	--	--	--	--	--	--
324	PS2(38)	168	164	Note 1	Note 1	164	168	--	--
325	PS2(37)	164	160	Note 1	Note 1	160	164	--	--
326	PS2(36)	160	156	Note 1	Note 1	156	160	--	--
327	PS2(35)	156	152	Note 1	Note 1	152	156	--	--
328	VCCA	--	--	--	--	--	--	--	--
329	PS2(34)	152	148	Note 1	Note 1	148	152	--	--
330	PS2(33)	148	144	Note 1	Note 1	144	148	--	--

TABLE 5-1 DC Parametrics for IPR VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
331	PS2(32)	144	140	Note 1	Note 1	140	144	--	--
332	VCC	--	--	--	--	--	--	--	--
333	VTT	--	--	--	--	--	--	--	--
334	PS1(23)	108	104	Note 1	Note 1	104	108	--	--
335	VCCA	--	--	--	--	--	--	--	--
336	PS1(22)	104	100	Note 1	Note 1	100	104	--	--
337	PS1(21)	100	96	Note 1	Note 1	96	100	--	--
338	PS1(20)	96	92	Note 1	Note 1	92	96	--	--
339	PS1(19)	92	88	Note 1	Note 1	88	92	--	--
340	VCCA	--	--	--	--	--	--	--	--
341	PS1(18)	88	84	Note 1	Note 1	84	88	--	--
342	PS1(17)	84	80	Note 1	Note 1	80	84	--	--
343	PS1(16)	80	76	Note 1	Note 1	76	80	--	--
344	GND1	--	--	--	--	--	--	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on IPR-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP003 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V. Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

1. TPLH1 -- This parameter measures the time to generate a pipeline control bit from the clock edge. Since the entire pipreline is contained within the IPR device, all delays should be similar. The control bit, PS1(23), exhibits the longest routing path and has the greatest element of parasitic delay. To make this measurement, the pipeline register must be selected for loading. This is accomplished by asserting initf and pipesel high, and by asserting ssel(0) ans ssel(1) low. WCS(23) should be asserted high prior to the clock edge. The test pattern which accomplishes the L->H transition on PS1(23) is vector 101. The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures the time to detect a parity error after a load of an erroneous word into the the pipeline register. The parity error signal, PERR, is replicated into a bus of three bits for the purposes of minimizing board delay. PERR(2) has the largest parasitic delay, and should show the slowest propagation time To make this measurement, the signal PARDIS should be asserted low, and PEVEN should be asserted high. The rising edge of the clock should force odd parity on the pipeline register. The parity detect logic time delay is not dependant upon the bit in error. The test pattern which accomplishes the L->H transition of PERR(2) is 3,211. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures the time required to generate the serial data out signal, SDOUT. This signal passes the serial shift chain from 1 device to the next. To make this mesurement, the signal SDIN must be clocked 112 times to reach the SDOUT position. The shift chain should be enabled by asserting SSEL(0) low, and SSEL(1) high. The test pattern which accomplishes the L->H transition of SDOUT is 3,187. The maximum acceptable value for this parameter is TBD nS.

4. TSET1 -- The parameter measures the minimum set up time on the STALL bus. This delay is in the critical path of the OBP80. The stall assertion must arrive and be set up at the IPR within the first 1/2 of the clock period. To make this measurement, the WCS data path should be connected to the pipeline register. This is done by asserting SSEL(0) and SSEL(1) low. The WCS inputs should be asserted such that a change in the pipeline register outputs can be detected if a load occurs. The stall bus is symetrical, but STALL(0) has the greatest parasitic delay. The clock edge should be adjusted within the vector period until a load occurs. The vector which accomplishes the L->H transition on STALL(0) is 5,948. The maximum acceptable value for this parameter is TBD nS.

5. TSET2 -- This parameter measures the minimum set up time on the WCS bus. This delay is in the critical path of the OBP80. The outputs of the control store RAMs must arrive and be set up at the IPR prior to the rising edge of the clock. To make this measurement, The WCS should be connected to the pipeline register. The clock edge should be adjusted within the vector period until the load of WCS(0) does not occur. The vector which accomplishes the L->H transistion on WCS(0) is 8. The maximum acceptable value for this parameter is TBD nS.

TABLE 5-2 AC Parametrics for IPR VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
334	TPLH1	101	PS1(23)	CLK, CLKN; 120, 121	TBD
257	TPLH2	3,211	PERR(2)	CLK, CLKN; 120, 121	TBD
284	TPLH3	3,187	SDOUT	CLK, CLKN; 120, 121	TBD
120	TSET1	5,948	CLK	STALL(0); 124	TBD
120	TSET2	8	CLK	WCS(0); 59	TBD
334	TPHL1	104	PS1(23)	CLK, CLKN; 120, 121	TBD
257	TPHL2	3,215	PERR(2)	CLK, CLKN; 120, 121	TBD
284	TPHL3	3,191	SDOUT	CLK, CLKN; 120, 121	TBD

6. APPENDIX B -- IPR VLSI Burn-In Circuit

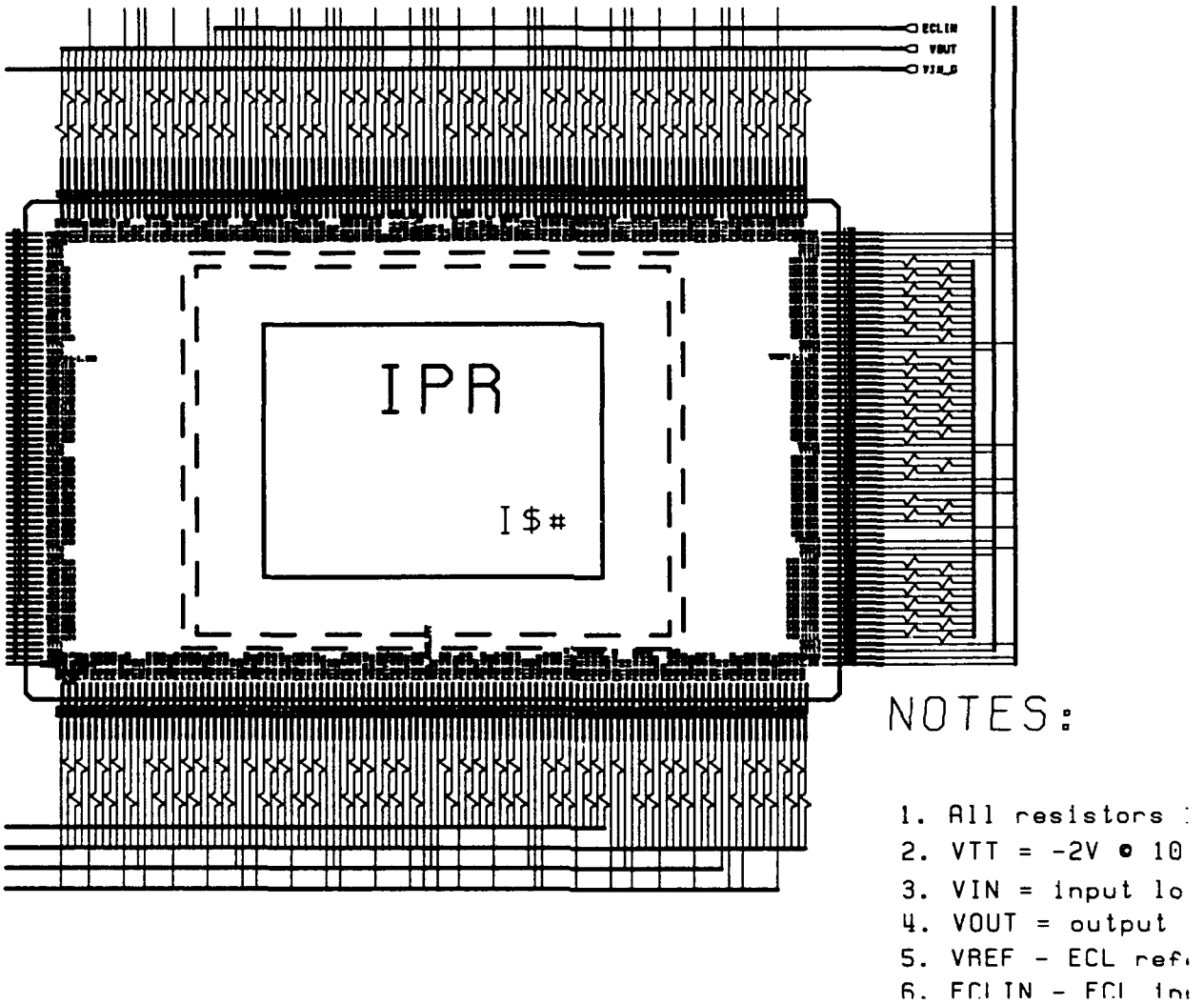

Figure 6-1 IPR VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- IPR VLSI Test Data Specification

All parametric data recorded on the IPR VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP004

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. **Sheet 0 shall not be furnished to supplier.**
2. **The 'Dash 2' configuration refers to the initial wafer run for design characterization only.**
3. **Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.**

PROGRAM AUTHORIZATION

Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION

Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

John R. Meadows

Principal Design Engineer

Rhonda K. Weaver

Full Custom Data Memory Controller for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP004	

SCALE	PAGE	SHEET
		0 of 42

Drawing Number: GOBP004

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	3/15/91	

											REV
		42	41	40	39	38	37	36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
											REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

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MARTIN MARIETTA CORPORATION

Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

John R. Meadows

Principal Design Engineer

Full Custom Data Memory Controller for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP004	

SCALE	PAGE	SHEET
		1 of 42

Drawing Number: GOBP004

REVISIONS				
REV	SH	DESCRIPTION	DATE	APPROVED

FSCM NO. 04236

	SIZE A	DRWG. NO. GOBP004	REV
	SCALE	PAGE	SHEET 2 of 42

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom DMC VLSI; hereinafter referred to as GOBP004, DMC, or part.

1.2 Part Number - The DMC VLSI shall be identified by the part number GOBP004.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Free-air Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP004-MT1	Magnetic media functional description of DMC VLSI
GOBP004-MT2	Magnetic media graphical description of DMC VLSI
GOBP004-MT3	Magnetic media assembly drawing of DMC VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the DMC VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP004-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP004-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP004-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the DMC VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the DMC VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

3.2.6.1 Total Dose - The DMC VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification are required to withstand 3E4 rads (Si) total dose and suffer no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Devices supplied to this specification shall not exhibit sustained latchup following exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec.

3.2.6.3 Single Particle Upset - Devices supplied to this specification shall exhibit an LET of 60 Mev/mg/cm^2 following exposure to a 3e-7 second pulse of ionizing radiation at a dose rate of 1e6 rad/sec.

3.2.6.4 Alternative Procedure for Single Event Upset - An alternative procedure for demonstrating compliance with the specification for Single Event Upset shall be no observable errors following:

A. Initialize the data storage elements with all one's.

B. Expose device to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec.

C. Interrogate the state of the device data storage elements.

D. Repeat Steps B and C with data storage elements set to all zeroes.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP004-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP004-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The DMC VLSI shall be packaged in a 256 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP004-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP004-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP004-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of DMC VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition E, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on DMC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 9. The pattern drivers should be connected, and forcing pattern number 9. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 1,452. The patterns drivers should be connected, and forcing pattern number 1,452. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on DMC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIH ECL 100K -- The ECL Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.2 V

3. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

4. VIL ECL 100K -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

5. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

6. IIH ECL 100K -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

7. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

8. IIL ECL 100K -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

9. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

10. VCD1N ECL 100K -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

    IOL = -3 mA, VTT = VCCA = VCC = 0 V.

11. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

12. VCD1P ECL 100K -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on DMC-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOL ECL 100K -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.6 V when the test is performed with the following parametric conditions:

   R_{LOAD} = 50 Ohm to VTT, VTT = -1.9 V, VCCA = VCC = 0 V.

3. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

4. VOH ECL 100K -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.6 V when the test is performed with the following parametric conditions:

   R_{LOAD} = 50 Ohm to VTT, VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

7. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

8. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

TABLE 5-1 DC Parametrics for DMC VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
1	VCC	--	--	--	--	--	--	--	--
2	VCCA	--	--	--	--	--	--	--	--
3	VCC	--	--	--	--	--	--	--	--
4	VTT	--	--	--	--	--	--	--	--
5	ADDR(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	ADDR(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
7	ADDR(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
8	ADDR(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
9	ADDR(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
10	ADDR(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
11	ADDR(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
12	ADDR(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
13	ADDR(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
14	ADDR(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
15	ADDR(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
16	ADDR(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
17	VCC	--	--	--	--	--	--	--	--
18	VTT	--	--	--	--	--	--	--	--
19	ADDR(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
20	ADDR(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
21	ADDR(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
22	DEST(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
23	DEST(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
24	DEST(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
25	DEST(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
26	DEST(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
27	DEST(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
28	DEST(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
29	DEST(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
30	DEST(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
31	DEST(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
32	VCC	--	--	--	--	--	--	--	--
33	VTT	--	--	--	--	--	--	--	--
34	DEST(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
35	DEST(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
36	DEST(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
37	DEST(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
38	DEST(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
39	DEST(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
40	MODE(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
41	MODE(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
42	EDCON(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
43	EDCON(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
44	EDCON(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
45	EDCON(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
46	DMS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
47	VCC	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	DMS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
50	DMS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
51	DMF(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
52	DMF(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
53	ABD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
54	ABD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
55	DM1CBS	--	--	Note 1	Note 1	--	--	Note 1	Note 1
56	DBD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
57	DBD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
58	DBD(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
59	DBD(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
60	DBD(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
61	VCC	--	--	--	--	--	--	--	--
62	VTT	--	--	--	--	--	--	--	--
63	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
64	VCC	--	--	--	--	--	--	--	--
65	BF(15)	183	146	Note 1	Note 1	146	183	--	--
66	BF(14)	183	146	Note 1	Note 1	146	183	--	--
67	BF(13)	183	146	Note 1	Note 1	146	183	--	--
68	BF(12)	183	146	Note 1	Note 1	146	183	--	--
69	VCCA	--	--	--	--	--	--	--	--
70	BF(11)	183	146	Note 1	Note 1	146	183	--	--
71	BF(10)	183	146	Note 1	Note 1	146	183	--	--
72	BF(9)	183	146	Note 1	Note 1	146	183	--	--
73	BF(8)	183	146	Note 1	Note 1	146	183	--	--
74	VCCA	--	--	--	--	--	--	--	--
75	BF(7)	183	146	Note 1	Note 1	146	183	--	--
76	VCC	--	--	--	--	--	--	--	--
77	VTT	--	--	--	--	--	--	--	--
78	BF(6)	183	146	Note 1	Note 1	146	183	--	--
79	BF(5)	183	146	Note 1	Note 1	146	183	--	--
80	BF(4)	183	146	Note 1	Note 1	146	183	--	--
81	VCCA	--	--	--	--	--	--	--	--
82	BF(3)	183	146	Note 1	Note 1	146	183	--	--
83	BF(2)	183	146	Note 1	Note 1	146	183	--	--
84	BF(1)	183	146	Note 1	Note 1	146	183	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
85	BF(0)	183	146	Note 1	Note 1	146	183	--	--
86	VCCA	--	--	--	--	--	--	--	--
87	VTT	--	--	--	--	--	--	--	--
88	VCC	--	--	--	--	--	--	--	--
89	DO1(21) ECL 100K	1323	1319	Note 1	Note 1	1319	1323	--	--
90	VCC	--	--	--	--	--	--	--	--
91	VTT	--	--	--	--	--	--	--	--
92	DO1(20) ECL 100K	19	15	Note 1	Note 1	15	19	--	--
93	VCCA	--	--	--	--	--	--	--	--
94	DO1(19) ECL 100K	67	22	Note 1	Note 1	22	67	--	--
95	DO1(18) ECL 100K	71	75	Note 1	Note 1	75	71	--	--
96	DO1(17) ECL 100K	23	19	Note 1	Note 1	19	23	--	--
97	DO1(16) ECL 100K	19	15	Note 1	Note 1	15	19	--	--
98	VCCA	--	--	--	--	--	--	--	--
99	DO1(15) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
100	DO1(14) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
101	DO1(13) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
102	DO1(12) ECL 100K	63	15	Note 1	Note 1	15	63	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
103	VCCA	--	--	--	--	--	--	--	--
104	VCC	--	--	--	--	--	--	--	--
105	VTT	--	--	--	--	--	--	--	--
106	DO1(11) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
107	DO1(10) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
108	DO1(9) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
109	DO1(8) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
110	VCCA	--	--	--	--	--	--	--	--
111	DO1(7) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
112	DO1(6) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
113	DO1(5) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
114	DO1(4) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
115	VCCA	--	--	--	--	--	--	--	--
116	DO1(3) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
117	DO1(2) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
118	VCC	--	--	--	--	--	--	--	--
119	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
120	DO1(1) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
121	DO1(0) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
122	VCCA	--	--	--	--	--	--	--	--
123	VCC	--	--	--	--	--	--	--	--
124	VCC	--	--	--	--	--	--	--	--
125	CLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
126	CLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
127	VCCA	--	--	--	--	--	--	--	--
128	VTT	--	--	--	--	--	--	--	--
129	VTT	--	--	--	--	--	--	--	--
130	VCC	--	--	--	--	--	--	--	--
131	DM1SIGN	539	491	Note 1	Note 1	491	539	--	--
132	VCC	--	--	--	--	--	--	--	--
133	VTT	--	--	--	--	--	--	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	MEMERR	715	707	Note 1	Note 1	707	715	--	--
136	BUSY(2)	723	719	Note 1	Note 1	719	723	--	--
137	BUSY(1)	723	719	Note 1	Note 1	719	723	--	--
138	BUSY(0)	723	719	Note 1	Note 1	719	723	--	--
139	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
140	WRF(3) ECL 100K	513	511	Note 1	Note 1	511	513	--	--
141	WRF(2) ECL 100K	513	511	Note 1	Note 1	511	513	--	--
142	WRF(1) ECL 100K	513	511	Note 1	Note 1	511	513	--	--
143	WRF(0) ECL 100K	513	511	Note 1	Note 1	511	513	--	--
144	VCCA	--	--	--	--	--	--	--	--
145	VTT	--	--	--	--	--	--	--	--
146	VCC	--	--	--	--	--	--	--	--
147	VTT	--	--	--	--	--	--	--	--
148	CSF(15) ECL 100K	1892	1895	Note 1	Note 1	1895	1892	--	--
149	CSF(14) ECL 100K	1901	1907	Note 1	Note 1	1907	1901	--	--
150	CSF(13) ECL 100K	1899	1901	Note 1	Note 1	1901	1899	--	--
151	VCCA	--	--	--	--	--	--	--	--
152	CSF(12) ECL 100K	740	756	Note 1	Note 1	740	756	--	--
153	CSF(11) ECL 100K	1876	1879	Note 1	Note 1	1879	1876	--	--
154	CSF(10) ECL 100K	1887	1891	Note 1	Note 1	1891	1887	--	--
155	CSF(9) ECL 100K	1883	1887	Note 1	Note 1	1887	1883	--	--
156	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
157	CSF(8) ECL 100K	728	740	Note 1	Note 1	740	728	--	--
158	CSF(7) ECL 100K	1860	1863	Note 1	Note 1	1863	1860	--	--
159	CSF(6) ECL 100K	1871	1875	Note 1	Note 1	1875	1871	--	--
160	VCC	--	--	--	--	--	--	--	--
161	VTT	--	--	--	--	--	--	--	--
162	CSF(5) ECL 100K	1867	1871	Note 1	Note 1	1871	1867	--	--
163	VCCA	--	--	--	--	--	--	--	--
164	CSF(4) ECL 100K	716	727	Note 1	Note 1	727	716	--	--
165	CSF(3) ECL 100K	259	303	Note 1	Note 1	303	259	--	--
166	CSF(2) ECL 100K	303	307	Note 1	Note 1	307	303	--	--
167	CSF(1) ECL 100K	255	259	Note 1	Note 1	255	259	--	--
168	VCCA	--	--	--	--	--	--	--	--
169	CSF(0) ECL 100K	307	255	Note 1	Note 1	255	307	--	--
170	VCC	--	--	--	--	--	--	--	--
171	VCC	--	--	--	--	--	--	--	--
172	VCC	--	--	--	--	--	--	--	--
173	VTT	--	--	--	--	--	--	--	--
174	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
175	VCC	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--
177	DEPTH	--	--	Note 1	Note 1	--	--	Note 1	Note 1
178	DI1(21) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
179	DI2(21) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
180	DI1(20) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
181	VREF (-1.3 V) ECL 100K	--	--	--	--	--	--	--	--
182	DI2(20) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
183	DI1(19) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
184	DI2(19) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
185	DI1(18) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
186	DI2(18) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
187	DI1(17) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
188	DI2(17) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
189	VCC	--	--	--	--	--	--	--	--
190	VTT	--	--	--	--	--	--	--	--
191	DI1(16) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
192	DI2(16) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
193	VREF (-1.3V) ECL 100K	--	--	--	--	--	--	--	--
194	DI1(15) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
195	DI2(15) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
196	DI1(14) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
197	DI2(14) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
198	DI1(13) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
199	DI2(13) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
200	DI1(12) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	DI2(12) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
202	DI1(11) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	DI2(11) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	VCC	--	--	--	--	--	--	--	--
205	VTT	--	--	--	--	--	--	--	--
206	VREF(-1.3V) ECL 100K	--	--	--	--	--	--	--	--
207	DI1(10) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
208	DI2(10) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	DI1(9) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
210	DI2(9) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
211	DI1(8) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
212	DI2(8) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	VREF(-1.3V) ECL 100K	--	--	--	--	--	--	--	--
214	DI1(7) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
215	DI2(7) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
216	DI1(6) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
217	DI2(6) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	DI1(5) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
219	VCC	--	--	--	--	--	--	--	--
220	VTT	--	--	--	--	--	--	--	--
221	DI2(5) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
222	DI1(4) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	DI2(4) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
224	DI1(3) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
225	DI2(3) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
226	DI1(2) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	DI2(2) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	DI1(1) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	DI2(1) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	DI1(0) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
231	DI2(0) ECL 100K	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	BFTST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VCC	--	--	--	--	--	--	--	--
234	VTT	--	--	--	--	--	--	--	--
235	VCCA	--	--	--	--	--	--	--	--
236	VCC	--	--	--	--	--	--	--	--
237	VCC	--	--	--	--	--	--	--	--
238	VTT	--	--	--	--	--	--	--	--
239	DMA(0) ECL 100K	295	247	Note 1	Note 1	247	295	--	--
240	DMA(1) ECL 100K	299	251	Note 1	Note 1	251	299	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
241	VCCA	--	--	--	--	--	--	--	--
242	DMA(2) ECL 100K	303	255	Note 1	Note 1	255	303	--	--
243	DMA(3) ECL 100K	307	259	Note 1	Note 1	259	307	--	--
244	DMA(4) ECL 100K	295	247	Note 1	Note 1	247	295	--	--
245	DMA(5) ECL 100K	299	251	Note 1	Note 1	251	299	--	--
246	VCCA	--	--	--	--	--	--	--	--
247	DMA(6) ECL 100K	303	255	Note 1	Note 1	255	303	--	--
248	VCC	--	--	--	--	--	--	--	--
249	VTT	--	--	--	--	--	--	--	--
250	DMA(7) ECL 100K	307	259	Note 1	Note 1	259	307	--	--
251	DMA(8) ECL 100K	295	247	Note 1	Note 1	247	295	--	--
252	DMA(9) ECL 100K	299	251	Note 1	Note 1	251	299	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	DMA(10) ECL 100K	303	255	Note 1	Note 1	255	303	--	--
255	DMA(11) ECL 100K	307	259	Note 1	Note 1	259	307	--	--
256	DMA(12) ECL 100K	295	247	Note 1	Note 1	247	295	--	--
257	DMA(13) ECL 100K	299	251	Note 1	Note 1	251	299	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
258	VCCA	--	--	--	--	--	--	--	--
259	DMA(14) ECL 100K	303	255	Note 1	Note 1	255	303	--	--
260	DMA(15) ECL 100K	307	259	Note 1	Note 1	259	307	--	--
261	VTT	--	--	--	--	--	--	--	--
262	VCC	--	--	--	--	--	--	--	--
263	VTT	--	--	--	--	--	--	--	--
264	VTT	--	--	--	--	--	--	--	--
265	VCCA	--	--	--	--	--	--	--	--
266	VTT	--	--	--	--	--	--	--	--
267	XSRC(0)	295	247	Note 1	Note 1	247	295	--	--
268	XSRC(1)	299	251	Note 1	Note 1	251	299	--	--
269	XSRC(2)	303	255	Note 1	Note 1	255	303	--	--
270	VCCA	--	--	--	--	--	--	--	--
271	XSRC(3)	307	259	Note 1	Note 1	259	307	--	--
272	XSRC(4)	295	247	Note 1	Note 1	247	295	--	--
273	XSRC(5)	299	251	Note 1	Note 1	251	299	--	--
274	XSRC(6)	303	255	Note 1	Note 1	252	303	--	--
275	VCCA	--	--	--	--	--	--	--	--
276	VCC	--	--	--	--	--	--	--	--
277	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
278	XSRC(7)	307	259	Note 1	Note 1	259	307	--	--
279	XSRC(8)	295	247	Note 1	Note 1	247	295	--	--
280	XSRC(9)	299	251	Note 1	Note 1	251	299	--	--
281	XSRC(10)	303	255	Note 1	Note 1	255	303	--	--
282	VCCA	--	--	--	--	--	--	--	--
283	XSRC(11)	307	259	Note 1	Note 1	259	307	--	--
284	VCC	--	--	--	--	--	--	--	--
285	XSRC(12)	295	247	Note 1	Note 1	247	295	--	--
286	XSRC(13)	299	251	Note 1	Note 1	251	299	--	--
287	VCCA	--	--	--	--	--	--	--	--
288	XSRC(14)	303	255	Note 1	Note 1	255	303	--	--
289	XSRC(15)	307	259	Note 1	Note 1	259	307	--	--
290	VCC	--	--	--	--	--	--	--	--
291	SEAL RING VTT	--	--	--	--	--	--	--	--
292	DO2(0) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
293	DO2(1) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
294	VCCA	--	--	--	--	--	--	--	--
295	DO2(2) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
296	DO2(3) ECL 100K	75	27	Note 1	Note 1	27	75	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
297	DO2(4) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
298	DO2(5) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
299	VCCA	--	--	--	--	--	--	--	--
300	DO2(6) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
301	DO2(7) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
302	DO2(8) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
303	DO2(9) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
304	VCC	--	--	--	--	--	--	--	--
305	VTT	--	--	--	--	--	--	--	--
306	VCCA	--	--	--	--	--	--	--	--
307	DO2(10) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
308	DO2(11) ECL 100K	75	27	Note 1	Note 1	27	75	--	--
309	DO2(12) ECL 100K	63	15	Note 1	Note 1	15	63	--	--
310	DO2(13) ECL 100K	67	19	Note 1	Note 1	19	67	--	--
311	VCCA	--	--	--	--	--	--	--	--
312	DO2(14) ECL 100K	71	23	Note 1	Note 1	23	71	--	--
313	DO2(15) ECL 100K	75	27	Note 1	Note 1	27	75	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
314	DO2(16) ECL 100K	19	15	Note 1	Note 1	15	19	--	--
315	DO2(17) ECL 100K	23	19	Note 1	Note 1	23	19	--	--
316	VCCA	--	--	--	--	--	--	--	--
317	DO2(18) ECL 100K	71	75	Note 1	Note 1	75	71	--	--
318	VCC	--	--	--	--	--	--	--	--
319	VTT	--	--	--	--	--	--	--	--
320	DO2(19) ECL 100K	67	22	Note 1	Note 1	22	67	--	--
321	DO2(20) ECL 100K	19	15	Note 1	Note 1	15	19	--	--
322	DO2(21) ECL 100K	1323	1319	Note 1	Note 1	1319	1323	--	--
323	VCCA	--	--	--	--	--	--	--	--
324	VCC	--	--	--	--	--	--	--	--
325	INITF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
326	BFSEL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
327	BFSEL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
328	VCCA	--	--	--	--	--	--	--	--
329	SBS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
330	SBS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
331	SBS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
332	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for DMC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
333	VTT	--	--	--	--	--	--	--	--
334	SBS(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
335	VCCA	--	--	--	--	--	--	--	--
336	SBS(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
337	STALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
338	STALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
339	STALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
340	VCCA	--	--	--	--	--	--	--	--
341	STALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
342	STALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
343	ADDR(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
344	GND1	--	--	--	--	--	--	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

In Table 5-1, the pins are listed sequentially from 1 to 344, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on DMC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP004 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V for both GaAs and ECL inputs.

1. TPLH1 -- This parameter measures the time to generate a chip select, following the load of new data into the DMA register. This parameter is measured on CSF(15). The delay on all CSF bits is expected to be uniform, since a PLA structure was used to perform the decode. A new CSF decode is driven by the rising edge trigger which loads the DMA register. The pattern which accomplishes the L->H transistion is 1,895. The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures another important timing feature in the OBP80 Working Store critical path. The WRF write enables have been broken into 4 identical channels to minimize the effects of board level capacitive loading on the memory strobe. The test vector for the H-L transition generates a negative going pulse based on the falling edge of the clock. This measures the time at which the write begins. The test vector for the L-H transition generates a rising edge based upon the rising edge of the clock. This identifies the time at which the write terminates. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures the address availability to Working Store.. The test vector for this parameter loads the DMA register on the rising edge of the clock. This data passes directly to the DMA outputs. The pattern which accomplishes the L->H transistion is 247, and the H-L transition occurs on 295. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- This parameter measures the data availability to Working Store.. The test vector for this parameter loads the DMDW register on the rising edge of the clock. This data passes directly to the DOUT1 or DOUT2 outputs. The largest timing delay will be found on the ECC generated pins, DOx(16) - DOx(21). These busses contain the same data, but are provided on opposite ends of the die to minimize board level capacitive loading on the data written to memory. The delays are expected to be identical, since the data generation occurs in the center of the chip. The pattern which accomplishes the L->H transistion is 1,319, and the H-L transition occurs on 1,323. The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures the data availability from Working Store. The test vector for this parameter loads the DMDR register on the rising edge of the clock. This data passes directly to the XSRC outputs. The pattern which accomplishes the L->H transistion is 259, and the H->L transition occurs on 307. The maximum acceptable value for this parameter is TBD nS.

6. TSET1 -- This parameter measures the time required to ECC decode the data read from memory. The test vector for this parameter loads the decoded result from the 22 bit DIN bus into the DMDR register. This parameter can only be measured by skewing the data availablility on test vector 478. The result of this skew can be seen in subsequent miscompares on the XSRC bus in pattern 479. The maximum acceptable value for this parameter is TBD nS.

Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

TABLE 5-2 AC Parametrics for DMC VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
148	TPLH1	1,895	CSF(15)	(CLK,CLKN);126,125	TBD
140	TPLH2	511	WRF(3)	(CLK,CLKN); 126,125	TBD
239	TPLH3	247	DMA(0)	(CLK,CLKN); 126,125	TBD
322	TPLH4	1,319	DO2(21)	(CLK,CLKN); 126,125	TBD
289	TPLH5	259	XSRC(15)	(CLK,CLKN); 126,125	TBD
148	TPHL1	1,892	CSF(15)	(CLK,CLKN); 126,125	TBD
140	TPHL2	513	WRF(3)	(CLK,CLKN); 126,125	TBD
239	TPHL3	295	DMA(0)	(CLK,CLKN); 126,125	TBD
322	TPHL4	1,323	DO2(21)	(CLK,CLKN); 126,125	TBD
289	TPHL5	307	XSRC(15)	(CLK,CLKN); 126,125	TBD
267	TSET1	478	CLK; 126	XSRC(0); 267	TBD

6. APPENDIX B -- DMC VLSI Burn-In Circuit

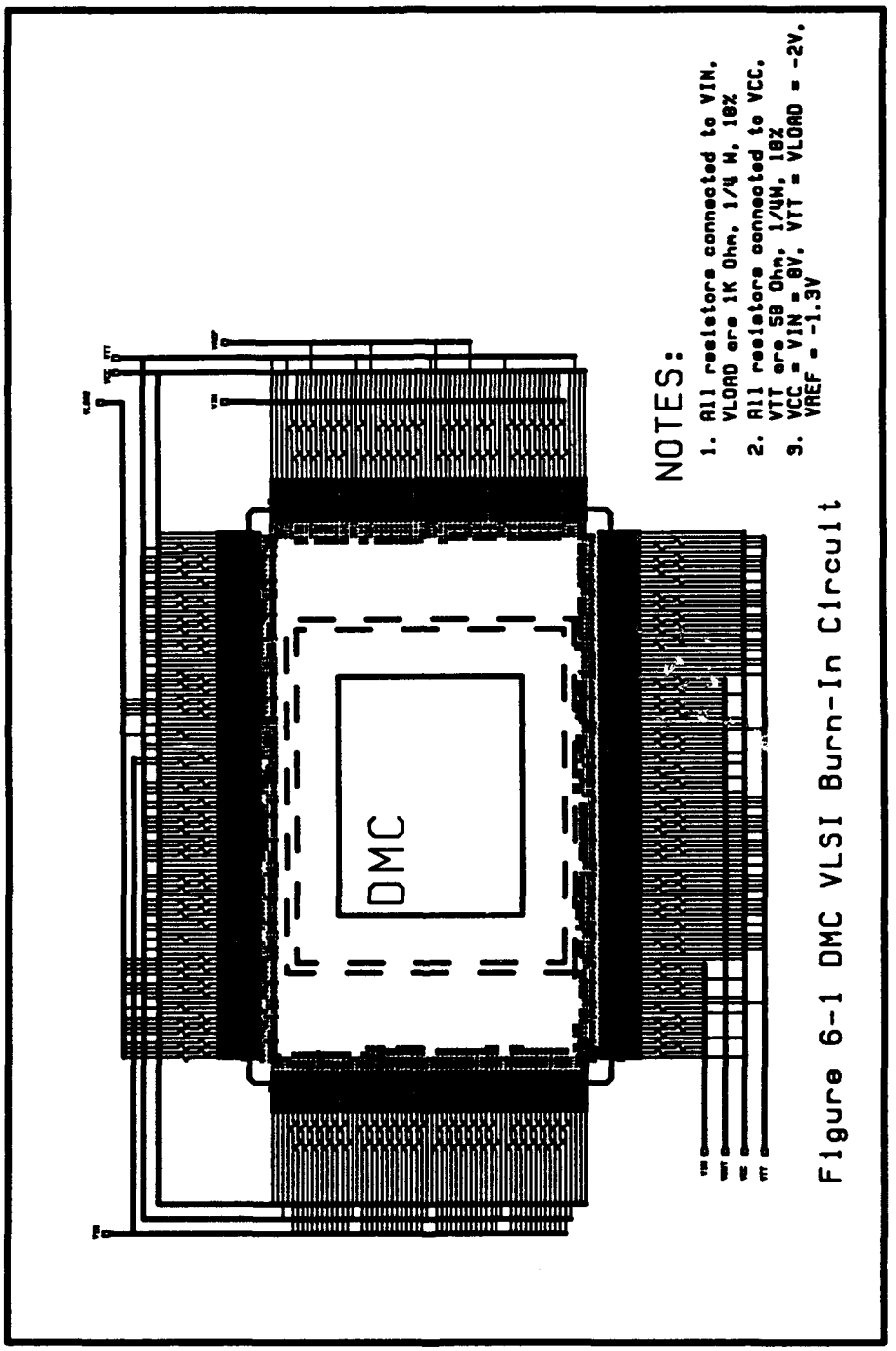

Figure 6-1 DMC VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- DMC VLSI Test Data Specification

All parametric data recorded on the DMC VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP005

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. **Sheet 0 shall not be furnished to supplier.**
2. **The 'Dash 2' configuration refers to the initial wafer run for design characterization only.**
3. **Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.**

PROGRAM AUTHORIZATION

Insertion Demonstrations of Digital Gallium Arsenide

Program Manager

Integrated Circuits Lead Engineer

Architectura Design Lead Engineer

Principal Design Engineer

MARTIN MARIETTA CORPORATION

Denver Division, P. O. Box 179, Denver Colorado,80201

Full Custom Timing and Interrupt Controller for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP005	

SCALE	PAGE	SHEET
		0 of 38

Drawing Number: GOBP005

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	7/31/91	

											REV
						38	37	36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
											REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

Insertion Demonstrations of Digital Gallium Arsenide

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FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP005	

SCALE	PAGE	SHEET
		1 of 38

Drawing Number: GOBP005

REVISIONS				
REV	SH	DESCRIPTION	DATE	APPROVED

FSCM NO. 04236

	SIZE	DRWG. NO.	REV
	A	GOBP005	
	SCALE	PAGE	SHEET 2 of 38

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom TIC VLSI; hereinafter referred to as GOBP005, TIC, or part.

1.2 Part Number - The TIC VLSI shall be identified by the part number GOBP005.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Free-air Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP005-MT1	Magnetic media functional description of TIC VLSI
GOBP005-MT2	Magnetic media graphical description of TIC VLSI
GOBP005-MT3	Magnetic media assembly drawing of TIC VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the TIC VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP005-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP005-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP005-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the TIC VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the TIC VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

3.2.6.1 Total Dose - The TIC VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification are required to withstand 3E4 rads (Si) total dose and suffer no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Devices supplied to this specification shall not exhibit sustained latchup following exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec.

3.2.6.3 Single Particle Upset - Devices supplied to this specification shall exhibit an LET of 60 Mev/mg/cm^2 following exposure to a 3e-7 second pulse of ionizing radiation at a dose rate of 1e6 rad/sec.

3.2.6.4 Alternative Procedure for Single Event Upset - An alternative procedure for demonstrating compliance with the specification for Single Event Upset shall be no observable errors following:

A. Initialize the data storage elements with all one's.

B. Expose device to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec.

C. Interrogate the state of the device data storage elements.

D. Repeat Steps B and C with data storage elements set to all zeroes.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP005-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP005-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The TIC VLSI shall be packaged in a 256 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP005-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP005-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP005-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High for Martin Marietta GaAs Level I/O's. For ECL Level outputs an output load of 50 Ohms to VTT shall be used. The Vil and Vih test input levels, and the Voh, Vol and threshold value, Vth test output comparison limits shall be varied to track the power supply variations.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of TIC VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition E, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on TIC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 235. The pattern drivers should be connected, and forcing pattern number 235. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 280. The patterns drivers should be connected, and forcing pattern number 280. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on TIC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

3. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

4. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on TIC-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V.

2. VOL ECL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.620 V when the test is performed with the following parametric conditions:

   Vin=Vih(max) or Vil(min)

3. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V.

4. VOH ECL -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -1.020 V when the test is performed with the following parametric conditions:

   Vin=Vih(max) or Vil(min)

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric

conditions:

IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

7. VCD1P ECL -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

8. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

9. IOSH ECL -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -50 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

10. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

    VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

In Table 5-1, the pins are listed sequentially from 1 to 256, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for TIC VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
1	VTT	--	--	--	--	--	--	--	--
2	VCC	--	--	--	--	--	--	--	--
3	WCS(6) ECL OUTPUT	7,763	7,747	Note 1	Note 1	7,747	7,747	--	--
4	WCS(7) ECL OUTPUT	7,859	7,763	Note 1	Note 1	7,763	7,763	--	--
5	WCS(8) ECL OUTPUT	7,875	7,859	Note 1	Note 1	7,859	7,875	--	--
6	VCCA	--	--	--	--	--	--	--	--
7	WCS(9) ECL OUTPUT	7,891	7,875	Note 1	Note 1	7,875	7,891	--	--
8	WCS(10) ECL OUTPUT	7,907	7,891	Note 1	Note 1	7,891	7,907	--	--
9	WCS(11) ECL OUTPUT	8,003	7,907	Note 1	Note 1	7,907	8,003	--	--
10	WCS(12) ECL OUTPUT	8,019	8,003	Note 1	Note 1	8,003	8,019	--	--
11	VCCA	--	--	--	--	--	--	--	--
12	WCS(13) ECL OUTPUT	8,035	8,019	Note 1	Note 1	8,019	8,035	--	--
13	WCS(14) ECL OUTPUT	8,051	8,035	Note 1	Note 1	8,035	8,051	--	--
14	WCS(15) ECL OUTPUT	8,147	8,051	Note 1	Note 1	8,051	8,147	--	--
15	WCS(16) ECL OUTPUT	8,163	8,147	Note 1	Note 1	8,147	8,163	--	--
16	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
17	VCC	--	--	--	--	--	--	--	--
18	VCCA	--	--	--	--	--	--	--	--
19	WCS(17) ECL OUTPUT	8,179	8,163	Note 1	Note 1	8,163	8,179	--	--
20	WCS(18) ECL OUTPUT	8,195	8,179	Note 1	Note 1	8,179	8,195	--	--
21	WCS(19) ECL OUTPUT	8,291	8,195	Note 1	Note 1	8,195	8,291	--	--
22	WCS(20) ECL OUTPUT	8,307	8,291	Note 1	Note 1	8,291	8,307	--	--
23	WCS(21) ECL OUTPUT	8,323	8,307	Note 1	Note 1	8,307	8,323	--	--
24	VCCA	--	--	--	--	--	--	--	--
25	WCS(22) ECL OUTPUT	8,339	8,323	Note 1	Note 1	8,323	8,339	--	--
26	WCS(23) ECL OUTPUT	8,435	8,339	Note 1	Note 1	8,339	8,435	--	--
27	WCS(24) ECL OUTPUT	8,451	8,435	Note 1	Note 1	8,435	8,451	--	--
28	WCS(25) ECL OUTPUT	8,467	8,451	Note 1	Note 1	8,451	8,467	--	--
29	VCCA	--	--	--	--	--	--	--	--
30	WCS(26) ECL OUTPUT	8,483	8,467	Note 1	Note 1	8,467	8,483	--	--
31	WCS(27) ECL OUTPUT	8,579	8,483	Note 1	Note 1	8,483	8,579	--	--
32	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
33	VCC	--	--	--	--	--	--	--	--
34	WCS(28) ECL OUTPUT	8,595	8,579	Note 1	Note 1	8,579	8,595	--	--
35	WCS(29) ECL OUTPUT	8,611	8,595	Note 1	Note 1	8,595	8,611	--	--
36	VCCA	--	--	--	--	--	--	--	--
37	WCS(30) ECL OUTPUT	8,627	8,611	Note 1	Note 1	8,611	8,627	--	--
38	WCS(31) ECL OUTPUT	8,723	8,627	Note 1	Note 1	8,627	8,723	--	--
39	WCS(32) ECL OUTPUT	8,739	8,723	Note 1	Note 1	8,723	8,739	--	--
40	WCS(33) ECL OUTPUT	8,755	8,739	Note 1	Note 1	8,739	8,755	--	--
41	VCCA	--	--	--	--	--	--	--	--
42	WCS(34) ECL OUTPUT	8,771	8,755	Note 1	Note 1	8,755	8,771	--	--
43	WCS(35) ECL OUTPUT	8,867	8,771	Note 1	Note 1	8,771	8,867	--	--
44	WCS(36) ECL OUTPUT	8,883	8,867	Note 1	Note 1	8,867	8,883	--	--
45	WCS(37) ECL OUTPUT	8,899	8,883	Note 1	Note 1	8,883	8,899	--	--
46	WCS(38) ECL OUTPUT	8,915	8,899	Note 1	Note 1	8,899	8,915	--	--
47	VCCA	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
49	VCC	--	--	--	--	--	--	--	--
50	WCS(39) ECL OUTPUT	9,011	8,915	Note 1	Note 1	8,915	9,011	--	--
51	WCS(40) ECL OUTPUT	9,027	9,011	Note 1	Note 1	9,011	9,027	--	--
52	WCS(41) ECL OUTPUT	9,043	9,027	Note 1	Note 1	9,027	9,043	--	--
53	WCS(42) ECL OUTPUT	9,059	9,043	Note 1	Note 1	9,043	9,059	--	--
54	VCCA	--	--	--	--	--	--	--	--
55	WCS(43) ECL OUTPUT	9,155	9,059	Note 1	Note 1	9,059	9,155	--	--
56	WCS(44) ECL OUTPUT	9,171	9,155	Note 1	Note 1	9,155	9,171	--	--
57	WCS(45) ECL OUTPUT	9,187	9,171	Note 1	Note 1	9,171	9,187	--	--
58	WCS(46) ECL OUTPUT	9,203	9,187	Note 1	Note 1	9,187	9,203	--	--
59	VCCA	--	--	--	--	--	--	--	--
60	WCS(47) ECL OUTPUT	9,299	9,203	Note 1	Note 1	9,203	9,299	--	--
61	WCS(48) ECL OUTPUT	9,315	9,299	Note 1	Note 1	9,299	9,315	--	--
62	WCS(49) ECL OUTPUT	9,331	9,315	Note 1	Note 1	9,315	9,331	--	--
63	VTT	--	--	--	--	--	--	--	--
64	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
65	WCS(50) ECL OUTPUT	9,347	9,331	Note 1	Note 1	9,331		--	--
66	WCS(51) ECL OUTPUT	9,443	9,347	Note 1	Note 1	9,347		--	--
67	VCC	--	--	--	--	--	--	--	--
68	VCCA	--	--	--	--	--	--	--	--
69	VTT	--	--	--	--	--	--	--	--
70	VCC	--	--	--	--	--	--	--	--
71	WCS(52) ECL OUTPUT	9,459	9,443	Note 1	Note 1	9,443	9,459	--	--
72	WCS(53) ECL OUTPUT	9,475	9,459	Note 1	Note 1	9,459	9,475	--	--
73	WCS(54) ECL OUTPUT	9,491	9,475	Note 1	Note 1	9,475	9,491	--	--
74	WCS(55) ECL OUTPUT	9,527	9,491	Note 1	Note 1	9,491	9,527	--	--
75	VCCA	--	--	--	--	--	--	--	--
76	VCCA	--	--	--	--	--	--	--	--
77	MCLK ECL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
78	MCLKN ECL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
79	VCC	--	--	--	--	--	--	--	--
80	VCC	--	--	--	--	--	--	--	--
81	MSYNC	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
82	VCC	--	--	--	--	--	--	--	--
83	CLK ECL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
84	CLKN ECL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
85	VCC	--	--	--	--	--	--	--	--
86	VCC	--	--	--	--	--	--	--	--
87	VTT	--	--	--	--	--	--	--	--
88	VCC	--	--	--	--	--	--	--	--
89	TDI	--	--	Note 1	Note 1	--	--	Note 1	Note 1
90	TMS	--	--	Note 1	Note 1	--	--	Note 1	Note 1
91	TRSTF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
92	TCLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
93	PSELF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
94	TDOIPR	--	--	Note 1	Note 1	--	--	Note 1	Note 1
95	TDOMCS	--	--	Note 1	Note 1	--	--	Note 1	Note 1
96	TDOC1	--	--	Note 1	Note 1	--	--	Note 1	Note 1
97	CLRF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
98	CMDCLRF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
99	CEX	--	--	Note 1	Note 1	--	--	Note 1	Note 1
100	CMP	--	--	Note 1	Note 1	--	--	Note 1	Note 1
101	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
102	STALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
103	STALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
104	STALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
105	SEAL RING VTT	--	--	--	--	--	--	--	--
106	VCC	--	--	--	--	--	--	--	--
107	STALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
108	STALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
109	VTT	--	--	--	--	--	--	--	--
110	VTT	--	--	--	--	--	--	--	--
111	VCC	--	--	--	--	--	--	--	--
112	VCC	--	--	--	--	--	--	--	--
113	VCCA	--	--	--	--	--	--	--	--
114	TDOEN	259	179	Note 1	Note 1	179	259	--	--
115	TDO	203	187	Note 1	Note 1	187	203	--	--
116	TDIC1	235	203	Note 1	Note 1	203	235	--	--
117	TDIIPR	235	203	Note 1	Note 1	203	235	--	--
118	TDIMCS	235	203	Note 1	Note 1	203	235	--	--
119	VCCA	--	--	--	--	--	--	--	--
120	VCC	--	--	--	--	--	--	--	--
121	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
122	VTT	--	--	--	--	--	--	--	--
123	VTT	--	--	--	--	--	--	--	--
124	VCC	--	--	--	--	--	--	--	--
125	VCCA	--	--	--	--	--	--	--	--
126	VCC	--	--	--	--	--	--	--	--
127	SCLK(0) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
128	SCLKN(0) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
129	VTT	--	--	--	--	--	--	--	--
130	VCC	--	--	--	--	--	--	--	--
131	VCCA	--	--	--	--	--	--	--	--
132	SCLK(1) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
133	SCLKN(1) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	SCLK(2) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
136	SCLKN(2) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
137	SCLK(3) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
138	SCLKN(3) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
139	VCCA	--	--	--	--	--	--	--	--
140	SCLK(4) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
141	SCLKN(4) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
142	SCLK(5) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
143	SCLKN(5) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
144	VTT	--	--	--	--	--	--	--	--
145	VCC	--	--	--	--	--	--	--	--
146	VCCA	--	--	--	--	--	--	--	--
147	VCC	--	--	--	--	--	--	--	--
148	SCLK(6) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
149	SCLKN(6) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
150	SCLK(7) ECL OUTPUT	25	19	Note 1	Note 1	19	25	--	--
151	SCLKN(7) ECL OUTPUT	19	25	Note 1	Note 1	25	19	--	--
152	VCCA	--	--	--	--	--	--	--	--
153	C1A(0)	775	619	Note 1	Note 1	619	775	--	--
154	C1B(0)	775	619	Note 1	Note 1	619	775	--	--
155	C1A(1)	2,091	2,087	Note 1	Note 1	2,087	2,091	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
156	C1B(1)	2,091	2,087	Note 1	Note 1	2,087	2,091	--	--
157	VCCA	--	--	--	--	--	--	--	--
158	C1A(2)	2,091	2,087	Note 1	Note 1	2,087	2,091	--	--
159	C1B(2)	2,091	2,087	Note 1	Note 1	2,087	2,091	--	--
160	VTT	--	--	--	--	--	--	--	--
161	VCC	--	--	--	--	--	--	--	--
162	C1A(3)	763	759	Note 1	Note 1	759	763	--	--
163	C1B(3)	763	759	Note 1	Note 1	759	763	--	--
164	VCCA	--	--	--	--	--	--	--	--
165	C1A(4)	683	679	Note 1	Note 1	679	683	--	--
166	C1B(4)	683	679	Note 1	Note 1	679	683	--	--
167	IPR(0)	1,451	1,447	Note 1	Note 1	1,447	1,451	--	--
168	IPR(1)	1,447	1,451	Note 1	Note 1	1,451	1,447	--	--
169	VCCA	--	--	--	--	--	--	--	--
170	IPR(2)	1,371	1,367	Note 1	Note 1	1,367	1,371	--	--
171	IPR(3)	1,699	1,695	Note 1	Note 1	1,695	1,695	--	--
172	VTT	--	--	--	--	--	--	--	--
173	PARDIS	7,151	7,295	Note 1	Note 1	7,295	7,151	--	--
174	STPINT	73	53	Note 1	Note 1	53	73	--	--
175	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
176	VTT	--	--	--	--	--	--	--	--
177	VCC	--	--	--	--	--	--	--	--
178	MCS(0)	1,011	1,007	Note 1	Note 1	1,007	1,011	--	--
179	MCS(1)	1,029	1,023	Note 1	Note 1	1,023	1,029	--	--
180	MCS(2)	339	335	Note 1	Note 1	335	339	--	--
181	MCS(3)	339	335	Note 1	Note 1	335	339	--	--
182	VCCA	--	--	--	--	--	--	--	--
183	MCS(4)	5,711	5,707	Note 1	Note 1	5,707	5,711	--	--
184	MCS(5)	1,119	963	Note 1	Note 1	963	1,119	--	--
185	INITF(0)	36	16	Note 1	Note 1	16	36	--	--
186	INITF(1)	36	16	Note 1	Note 1	16	36	--	--
187	VCCA	--	--	--	--	--	--	--	--
188	INITF(2)	36	16	Note 1	Note 1	16	36	--	--
189	WHOA(0)	4,199	3,903	Note 1	Note 1	3,903	4,199	--	--
190	WHOA(1)	4,199	3,903	Note 1	Note 1	3,903	4,199	--	--
191	VTT	--	--	--	--	--	--	--	--
192	VCC	--	--	--	--	--	--	--	--
193	WHOA(2)	4,199	3,903	Note 1	Note 1	3,903	4,199	--	--
194	MPYLD	53	73	Note 1	Note 1	73	53	--	--
195	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
196	VCCA	--	--	--	--	--	--	--	--
197	VTT	--	--	--	--	--	--	--	--
198	VCC	--	--	--	--	--	--	--	--
199	VTT	--	--	--	--	--	--	--	--
200	VCC	--	--	--	--	--	--	--	--
201	VCC	--	--	--	--	--	--	--	--
202	BF	9,556	9,540	Note 1	Note 1	9,540	9,556	--	--
203	VCCA	--	--	--	--	--	--	--	--
204	VCC	--	--	--	--	--	--	--	--
205	VCC	--	--	--	--	--	--	--	--
206	VCC	--	--	--	--	--	--	--	--
207	TST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
208	BFTST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	VTT	--	--	--	--	--	--	--	--
210	VTT	--	--	--	--	--	--	--	--
211	VCC	--	--	--	--	--	--	--	--
212	VCC	--	--	--	--	--	--	--	--
213	VCC	--	--	--	--	--	--	--	--
214	VTT	--	--	--	--	--	--	--	--
215	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
216	VCC	--	--	--	--	--	--	--	--
217	VTT	--	--	--	--	--	--	--	--
218	VTT	--	--	--	--	--	--	--	--
219	VCC	--	--	--	--	--	--	--	--
220	VCC	--	--	--	--	--	--	--	--
221	VCC	--	--	--	--	--	--	--	--
222	VTT	--	--	--	--	--	--	--	--
223	VTT	--	--	--	--	--	--	--	--
224	VTT	--	--	--	--	--	--	--	--
225	VTT	--	--	--	--	--	--	--	--
226	VTT	--	--	--	--	--	--	--	--
227	VTT	--	--	--	--	--	--	--	--
228	VCC	--	--	--	--	--	--	--	--
229	VCC	--	--	--	--	--	--	--	--
230	VCC	--	--	--	--	--	--	--	--
231	VTT	--	--	--	--	--	--	--	--
232	VTT	--	--	--	--	--	--	--	--
233	VTT	--	--	--	--	--	--	--	--
234	VCC	--	--	--	--	--	--	--	--
235	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
236	VCC	--	--	--	--	--	--	--	--
237	VCC	--	--	--	--	--	--	--	--
238	VCC	--	--	--	--	--	--	--	--
239	VTT	--	--	--	--	--	--	--	--
240	VTT	--	--	--	--	--	--	--	--
241	WCSWRF(0) ECL OUTPUT	7,647	7,651	Note 1	Note 1	7,651	7,647	--	--
242	WCSWRF(1) ECL OUTPUT	2,479	2,848	Note 1	Note 1	2,848	2,479	--	--
243	VCC	--	--	--	--	--	--	--	--
244	VCC	--	--	--	--	--	--	--	--
245	VCC	--	--	--	--	--	--	--	--
246	VCCA	--	--	--	--	--	--	--	--
247	WCS(0) ECL OUTPUT	7,587	7,571	Note 1	Note 1	7,571	7,587	--	--
248	WCS(1) ECL OUTPUT	7,603	7,587	Note 1	Note 1	7,587	7,603	--	--
249	WCS(2) ECL OUTPUT	7,619	7,603	Note 1	Note 1	7,603	7,619	--	--
250	WCS(3) ECL OUTPUT	7,715	7,619	Note 1	Note 1	7,619	7,715	--	--
251	VTT	--	--	--	--	--	--	--	--
252	VCC	--	--	--	--	--	--	--	--
253	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for TIC VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
254	VCC	--	--	--	--	--	--	--	--
255	WCS(4) ECL OUTPUT	7,731	7,715	Note 1	Note 1	7,715	7,731	--	--
256	WCS(5) ECL OUTPUT	7,747	7,731	Note 1	Note 1	7,731	7,747	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on TIC-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP005 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V.

1. TPLH1 -- This parameter measures the time to propagate a signal directly from the CEX input, through 4 levels of logic gating, and out the WHOA(0) output. This parameter is important because the GaAs level WHOA bus is used to stall the OBP80. These signals must be stable within the first one-half of a clock period.The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures the time needed to produce the MPYLD signal. This signal provides stall control to the MPY VLSI device, which does not have its own 'on-board' stall logic. Subsequent to the clock edge, the signal passes through two levels of logic before emerging out the GaAs level MPYLD pin. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures the time from clock edge to WCS(0). This test defines WCS(0) from the serial data path. The clock edge produces new contents for the WCS register, which is passed directly to the ECL level WCS(0) pin. A branch of the clock tree is reserved just to produce the WCS outputs. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- This parameter measures the time from the clock edge to the IPR(3) output. The signal must pass from the register outputs, through a Programmable Logic Array, and then emerges out the GaAs level IPR(3) pin.The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures the time to produce the positive half of the differential clock signal, SCLK(1). This clock is used to drive one of the two COMM1 VLSI devices. All VLSI device clocks are derived from the master oscillator. The differential master ECL level input clock is diveded by two, buffered, and passed to the ECL level SCLK(1) output.The maximum acceptable value for this parameter is TBD nS.

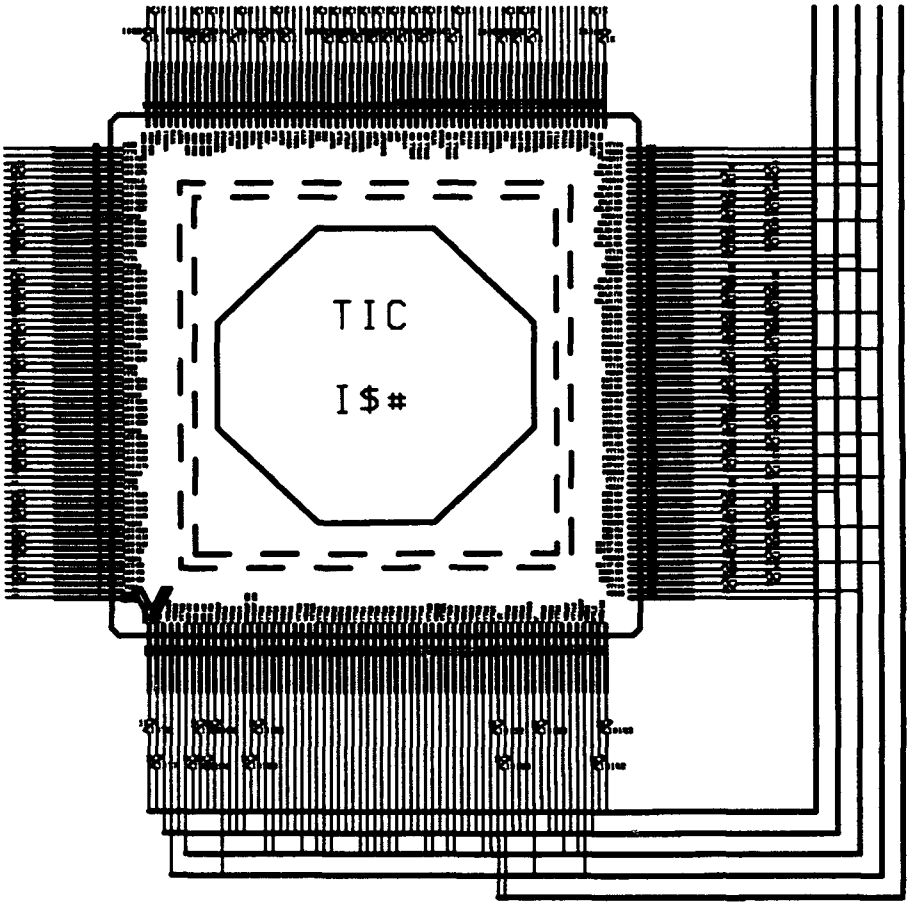
6. TPLH6 -- This parameter is used in conjunction with TPLH5 to determine VLSI device clock skew. The parameter measures the time to produce the negative half of the differential clock signal, SCLKN(1). This clock is used to drive the same COMM1 VLSI chip as TPLH5. This signal is derived from the same edge of the master clock, MCLK, MCLKN. The maximum acceptable value for this parameter is TBD nS.

Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

TABLE 5-2 AC Parametrics for TIC VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
189	TPLH1	3,905	WHOA(0)	CEX; 99	TBD
194	TPLH2	4,203	MPYLD	(CLK,CLKN); 83,84	TBD
247	TPLH3	2,405	WCS(0)	(CLK, CLKN); 83,84	TBD
171	TPLH4	3,073	IPR(3)	(CLK,CLKN); 83,84	TBD
127	TPLH5	21	SCLK(0)	(MCLK,MCLKN); 77,78	TBD
128	TPLH6	25	SCLKN(0)	(MCLK, MCLKN); 77,78	TBD
189	TPHL1	4,201	WHOA(0)	CEX; 99	TBD
194	TPHL2	3,907	MPYLD	(CLK,CLKN); 83,84	TBD
247	TPHL3	2,421	WCS(0)	(CLK,CLKN); 83,84	TBD
171	TPHL4	3,077	IPR(3)	(CLK,CLKN); 83,84	TBD
127	TPHL5	25	SCLK(0)	(MCLK,MCLKN); 77,78	TBD
128	TPHL6	21	SCLKN(0)	(MCLK,MCLKN); 77,78	TBD

6. APPENDIX B -- TIC VLSI Burn-In Circuit



NOTES:

1. All resistor
2. VTT = -2V ±
3. VIN = input
4. VOUT = outpu

ure 6-1, TIC VLSI Burn-In Circuit

Figure 6-1 TIC VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- TIC VLSI Test Data Specification

All parametric data recorded on the TIC VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP006

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. **Sheet 0 shall not be furnished to supplier.**
2. **The 'Dash 2' configuration refers to the initial wafer run for design characterization only.**
3. **Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.**

PROGRAM AUTHORIZATION

Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION

Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Principal Design Engineer

Full Custom Communications and Backplane Interface Device for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP006	

SCALE	PAGE	SHEET
		0 of 38

Drawing Number: GOBP006

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	7/11/91	

											REV
								36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
											REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

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Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer

Douglas N. Kreming

Principal Design Engineer

Rhonda L. Weaver

Full Custom Communications and Backplane Interface Device for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP006	

SCALE	PAGE	SHEET
		1 of 38

Drawing Number: GOBP006

REVISIONS				
REV	SH	DESCRIPTION	DATE	APPROVED

FSCM NO. 04236

	SIZE A	DRWG. NO. GOBP006	REV
	SCALE	PAGE	SHEET 2 of 38

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom COMM1 VLSI; hereinafter referred to as GOBP006, COMM1, or part.

1.2 Part Number - The COMM1 VLSI shall be identified by the part number GOBP006.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Free-air Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP006-MT1	Magnetic media functional description of COMM1 VLSI
GOBP006-MT2	Magnetic media graphical description of COMM1 VLSI
GOBP006-MT3	Magnetic media assembly drawing of COMM1 VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the COMM1 VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP006-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP006-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP006-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the COMM1 VLSI are as defined in the Table 2, DC Performance Characteristics of Appendix A.

3.2.5 AC Characteristics - The AC operating characteristics of the COMM1 VLSI are as defined in the Table 1, AC Performance Characteristics of Appendix A.

3.2.6 Radiation Resistance

3.2.6.1 Total Dose - The COMM1 VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification are required to withstand 3E4 rads (Si) total dose and suffer no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Devices supplied to this specification shall not exhibit sustained latchup following exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec.

3.2.6.3 Single Particle Upset - Devices supplied to this specification shall exhibit an LET of 60 Mev/mg/cm^2 following exposure to a 3e-7 second pulse of ionizing radiation at a dose rate of 1e6 rad/sec.

3.2.6.4 Alternative Procedure for Single Event Upset - An alternative procedure for demonstrating compliance with the specification for Single Event Upset shall be no observable errors following:

A. Initialize the data storage elements with all one's.

B. Expose device to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec.

C. Interrogate the state of the device data storage elements.

D. Repeat Steps B and C with data storage elements set to all zeroes.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP006-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP006-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The COMM1 VLSI shall be packaged in a 256 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP006-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP006-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP006-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 7.0 mA for Output Low and -0.8 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of COMM1 VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition E, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on COMM1-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 0- 8. The pattern drivers should be connected, and forcing pattern number 8. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V, PLUS5 = 5.5 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 0 - 10,156. The patterns drivers should be connected, and forcing pattern number 10,156. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

The following parameters have been defined for the input pins on COMM1-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 1.1 V.

2. VIH TTL -- The TTL Input High voltage. Pass criteria shall be VIH_{MIN} = 2.0 V.

3. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V.

4. VIL TTL -- The TTL Input Low Voltage. Pass criteria shall be VIL_{MAX} = 0.4 V.

5. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

6. IIH TTL -- The TTL Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -2.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = 2.0 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

7. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

8. IIL TTL-- The TTL Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +420 uA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = 0.4 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

9. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

10. VCD1N TTL -- The TTL Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

    IOL = -3 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

11. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

    NOTE: There is no TTL posiitive clamp diode, so no VCD1P test should be performed for those inputs.

The following parametric tests are defined for the output pins on COMM1-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0, PLUS5 =5.5 V.

2. VOL TTL -- The TTL Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.8 V when the test is performed with the following parametric conditions:

   IOL = +14 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

3. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 5.5V.

4. VOH TTL -- The TTL Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.8 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -1.9 V, VCCA = VCC = 0 V, PLUS5 = 4.5 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = PLUS5 = 0 V.

7. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

8. IOSH TTL -- The TTL Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = 0.0 V, VTT = -2.1 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

9. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

   VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

10. IOSL TTL -- The TTL Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric conditions:

    VTT = -1.9 V, VOH = 5.5 V, VCCA = VCC = 0 V, PLUS5 = 5.5 V.

    In Table 5-1, the pins are listed sequentially from 1 to 256, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for COMM1 VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
1	VTT	--	--	--	--	--	--	--	--
2	VCC	--	--	--	--	--	--	--	--
3	GSTALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
4	GSTALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
5	GSTALL(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	VCCA	--	--	--	--	--	--	--	--
7	GO0(0)	11	15	Note 1	Note 1	15	11	--	--
8	GO0(1)	227	231	Note 1	Note 1	231	227	--	--
9	GO0(2)	275	279	Note 1	Note 1	279	275	--	--
10	GO0(3)	323	327	Note 1	Note 1	327	323	--	--
11	VCCA	--	--	--	--	--	--	--	--
12	GO0(4)	371	375	Note 1	Note 1	375	371	--	--
13	GO0(5)	419	423	Note 1	Note 1	423	419	--	--
14	GO0(6)	467	471	Note 1	Note 1	471	467	--	--
15	GO0(7)	515	519	Note 1	Note 1	519	515	--	--
16	VTT	--	--	--	--	--	--	--	--
17	VCC	--	--	--	--	--	--	--	--
18	VCCA	--	--	--	--	--	--	--	--
19	GO0(8)	563	567	Note 1	Note 1	567	563	--	--
20	GO0(9)	611	615	Note 1	Note 1	615	611	--	--
21	GO0(10)	659	663	Note 1	Note 1	663	659	--	--

TABLE 5-1 DC Parame[illegible]r COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
22	GO0(11)	707	711	Note 1	Note 1	711	707	--	--
23	GO0(12)	755	759	Note 1	Note 1	759	755	--	--
24	VCCA	--	--	--	--	--	--	--	--
25	GO0(13)	803	807	Note 1	Note 1	807	803	--	--
26	GO0(14)	851	856	Note 1	Note 1	856	851	--	--
27	GO0(15)	899	903	Note 1	Note 1	903	899	--	--
28	GO0(16)	947	951	Note 1	Note 1	951	947	--	--
29	VCCA	--	--	--	--	--	--	--	--
30	GO1(0)	1264	1268	Note 1	Note 1	1268	1264	--	--
31	GO1(1)	1272	1276	Note 1	Note 1	1276	1272	--	--
32	VTT	--	--	--	--	--	--	--	--
33	VCC	--	--	--	--	--	--	--	--
34	TO0(0) TTL OUTPUT	1530	1456	Note 1	Note 1	1456	1530	--	--
35	TO0(1) TTL OUTPUT	1578	1456	Note 1	Note 1	1456	1578	--	--
36	PLUS5	--	--	--	--	--	--	--	--
37	TO0(2) TTL OUTPUT	1626	1456	Note 1	Note 1	1456	1626	--	--
38	TO0(3) TTL OUTPUT	1674	1456	Note 1	Note 1	1456	1674	--	--
39	TO0(4) TTL OUTPUT	1786	1456	Note 1	Note 1	1456	1786	--	--
40	TO0(5) TTL OUTPUT	1834	1456	Note 1	Note 1	1456	1834	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
41	PLUS5	--	--	--	--	--	--	--	--
42	TO0(6) TTL OUTPUT	1886	1456	Note 1	Note 1	1456	1886	--	--
43	TO0(7) TTL OUTPUT	1930	1456	Note 1	Note 1	1456	1930	--	--
44	TO0(8) TTL OUTPUT	2103	2099	Note 1	Note 1	2099	2103	--	--
45	TO0(9) TTL OUTPUT	2099	2103	Note 1	Note 1	2103	2099	--	--
46	TO0(10) TTL OUTPUT	2099	2103	Note 1	Note 1	2103	2099	--	--
47	PLUS5	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	VCC	--	--	--	--	--	--	--	--
50	TO0(11) TTL OUTPUT	2103	2099	Note 1	Note 1	2099	2103	--	--
51	TO0(12) TTL OUTPUT	2295	2291	Note 1	Note 1	2291	2295	--	--
52	TO0(13) TTL OUTPUT	2291	2295	Note 1	Note 1	2295	2291	--	--
53	TO0(14) TTL OUTPUT	2291	2295	Note 1	Note 1	2295	2291	--	--
54	PLUS5	--	--	--	--	--	--	--	--
55	TO0(15) TTL OUTPUT	2295	2291	Note 1	Note 1	2291	2295	--	--
56	TO0(16) TTL OUTPUT	2483	2487	Note 1	Note 1	2487	2483	--	--
57	TO0(17) TTL OUTPUT	2531	2535	Note 1	Note 1	2535	2531	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
58	TO0(18) TTL OUTPUT	2579	2583	Note 1	Note 1	2583	2579	--	--
59	PLUS5	--	--	--	--	--	--	--	--
60	TO0(19) TTL OUTPUT	2627	2631	Note 1	Note 1	2631	2627	--	--
61	TO0(20) TTL OUTPUT	2675	2679	Note 1	Note 1	2679	2675	--	--
62	TO0(21) TTL OUTPUT	2771	2775	Note 1	Note 1	2775	2771	--	--
63	VTT	--	--	--	--	--	--	--	--
64	VCC	--	--	--	--	--	--	--	--
65	TO0(22) TTL OUTPUT	2819	2823	Note 1	Note 1	2823	2819	--	--
66	TO0(23) TTL OUTPUT	2963	2967	Note 1	Note 1	2967	2963	--	--
67	VCCA	--	--	--	--	--	--	--	--
68	PLUS5	--	--	--	--	--	--	--	--
69	VTT	--	--	--	--	--	--	--	--
70	VCC	--	--	--	--	--	--	--	--
71	VCCA	--	--	--	--	--	--	--	--
72	PLUS5	--	--	--	--	--	--	--	--
73	TO0(24) TTL OUTPUT	3011	3015	Note 1	Note 1	3015	3011	--	--
74	TO0(25) TTL OUTPUT	3059	3063	Note 1	Note 1	3063	3059	--	--
75	TO0(26) TTL OUTPUT	3107	3111	Note 1	Note 1	3111	3107	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
76	TO0(27) TTL OUTPUT	3155	3159	Note 1	Note 1	3159	3155	--	--
77	VTT	--	--	--	--	--	--	--	--
78	VTT	--	--	--	--	--	--	--	--
79	VTT	--	--	--	--	--	--	--	--
80	VCC	--	--	--	--	--	--	--	--
81	VCC	--	--	--	--	--	--	--	--
82	PLUS5	--	--	--	--	--	--	--	--
83	TI0(16) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
84	TI0(15) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
85	TI0(14) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
86	TI0(13) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
87	VTT	--	--	--	--	--	--	--	--
88	VCC	--	--	--	--	--	--	--	--
89	TI0(12) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
90	TI0(11) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
91	TI0(10) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
92	TI0(9) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
93	TI0(8) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
94	TI0(7) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
95	TI0(6) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
96	TI0(5) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
97	TI0(4) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
98	TI0(3) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
99	TI0(2) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
100	TI0(1) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
101	TI0(0) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
102	TI1(1) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
103	TI1(0) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
104	TI2(3) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
105	SEAL RING VTT	--	--	--	--	--	--	--	--
106	VCC	--	--	--	--	--	--	--	--
107	TI2(2) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
108	TI2(1) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
109	TI2(0) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
110	TI3(1) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
111	TI3(0) TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
112	TCLRSTF TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
113	TCLK40 TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
114	TSYNC TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
115	TERR TTL INPUT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
116	PLUS5	--	--	--	--	--	--	--	--
117	VTT	--	--	--	--	--	--	--	--
118	VCC	--	--	--	--	--	--	--	--
119	VCC	--	--	--	--	--	--	--	--
120	VCC	--	--	--	--	--	--	--	--
121	VTT	--	--	--	--	--	--	--	--
122	VTT	--	--	--	--	--	--	--	--
123	VTT	--	--	--	--	--	--	--	--
124	VCC	--	--	--	--	--	--	--	--
125	PLUS5	--	--	--	--	--	--	--	--
126	VCCA	--	--	--	--	--	--	--	--
127	TO1(0) TTL OUTPUT	5173	5177	Note 1	Note 1	5177	5173	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
128	TO1(1) TTL OUTPUT	5189	5193	Note 1	Note 1	5193	5189	--	--
129	VTT	--	--	--	--	--	--	--	--
130	VCC	--	--	--	--	--	--	--	--
131	TO1(2) TTL OUTPUT	5205	5209	Note 1	Note 1	5209	5205	--	--
132	TO1(3) TTL OUTPUT	5221	5225	Note 1	Note 1	5225	5221	--	--
133	TO1(4) TTL OUTPUT	5237	5241	Note 1	Note 1	5241	5237	--	--
134	PLUS5	--	--	--	--	--	--	--	--
135	TO1(5) TTL OUTPUT	5253	5257	Note 1	Note 1	5257	5253	--	--
136	TO1(6) TTL OUTPUT	5269	5273	Note 1	Note 1	5273	5269	--	--
137	TO1(7) TTL OUTPUT	5285	5289	Note 1	Note 1	5289	5285	--	--
138	TO1(8) TTL OUTPUT	5301	5305	Note 1	Note 1	5305	5301	--	--
139	PLUS5	--	--	--	--	--	--	--	--
140	TO1(9) TTL OUTPUT	5317	5321	Note 1	Note 1	5321	5317	--	--
141	TO1(10) TTL OUTPUT	5333	5337	Note 1	Note 1	5337	5333	--	--
142	TO1(11) TTL OUTPUT	5349	5353	Note 1	Note 1	5353	5349	--	--
143	TO1(12) TTL OUTPUT	5365	5369	Note 1	Note 1	5369	5365	--	--
144	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
145	VCC	--	--	--	--	--	--	--	--
146	PLUS5	--	--	--	--	--	--	--	--
147	TO1(13) TTL OUTPUT	5381	5385	Note 1	Note 1	5385	5381	--	--
148	TO1(14) TTL OUTPUT	5397	5401	Note 1	Note 1	5401	5397	--	--
149	TO1(15) TTL OUTPUT	5413	5417	Note 1	Note 1	5417	5413	--	--
150	TO2(0) TTL OUTPUT	6257	6305	Note 1	Note 1	6305	6257	--	--
151	TO2(1) TTL OUTPUT	6273	6305	Note 1	Note 1	6305	6273	--	--
152	PLUS5	--	--	--	--	--	--	--	--
153	TO2(2) TTL OUTPUT	6289	6305	Note 1	Note 1	6305	6289	--	--
154	TO2(3) TTL OUTPUT	6289	6305	Note 1	Note 1	6305	6289	--	--
155	TO2(4) TTL OUTPUT	6321	6305	Note 1	Note 1	6305	6321	--	--
156	TO2(5) TTL OUTPUT	6321	6337	Note 1	Note 1	6337	6321	--	--
157	PLUS5	--	--	--	--	--	--	--	--
158	TCLRF TTL OUTPUT	15786	15790	Note 1	Note 1	15790	15786	--	--
159	TCLK10 TTL OUTPUT	22	26	Note 1	Note 1	26	22	--	--
160	VTT	--	--	--	--	--	--	--	--
161	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
162	VTT	--	--	--	--	--	--	--	--
163	VTT	--	--	--	--	--	--	--	--
164	VCCA	--	--	--	--	--	--	--	--
165	GERR	11685	11689	Note 1	Note 1	11689	11685	--	--
166	GO3(0)	1407	1411	Note 1	Note 1	1411	1407	--	--
167	GO3(1)	1399	1403	Note 1	Note 1	1403	1399	--	--
168	GO3(2)	1399	1403	Note 1	Note 1	1403	1399	--	--
169	VCCA	--	--	--	--	--	--	--	--
170	GO2(0)	1327	1331	Note 1	Note 1	1331	1327	--	--
171	GO2(1)	1331	1335	Note 1	Note 1	1335	1331	--	--
172	GO2(2)	1335	1339	Note 1	Note 1	1339	1335	--	--
173	GO2(3)	1339	1343	Note 1	Note 1	1343	1339	--	--
174	GCMP	6958	6954	Note 1	Note 1	6958	6954	--	--
175	VCCA	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--
177	VCC	--	--	--	--	--	--	--	--
178	GSDO	6974	6978	Note 1	Note 1	6978	6974	--	--
179	GBUSY(0)	7578	7582	Note 1	Note 1	7582	7578	--	--
180	GBUSY(1)	7578	7582	Note 1	Note 1	7582	7578	--	--
181	GBUSY(2)	7578	7582	Note 1	Note 1	7582	7578	--	--

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
182	VCCA	--	--	--	--	--	--	--	--
183	VCC	--	--	--	--	--	--	--	--
184	VCC	--	--	--	--	--	--	--	--
185	GI3	--	--	Note 1	Note 1	--	--	Note 1	Note 1
186	GSELCMP	--	--	Note 1	Note 1	--	--	Note 1	Note 1
187	VCCA	--	--	--	--	--	--	--	--
188	GPLDCMP	--	--	Note 1	Note 1	--	--	Note 1	Note 1
189	GSLDCMP	--	--	Note 1	Note 1	--	--	Note 1	Note 1
190	GSSELX	--	--	Note 1	Note 1	--	--	Note 1	Note 1
191	VTT	--	--	--	--	--	--	--	--
192	VCC	--	--	--	--	--	--	--	--
193	GLDX	--	--	Note 1	Note 1	--	--	Note 1	Note 1
194	GSDI	--	--	Note 1	Note 1	--	--	Note 1	Note 1
195	VCC	--	--	--	--	--	--	--	--
196	VCCA	--	--	--	--	--	--	--	--
197	VTT	--	--	--	--	--	--	--	--
198	VCC	--	--	--	--	--	--	--	--
199	GCLRF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
200	GMODE	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	GI2(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
202	GI2(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	GI2(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	GI2(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
205	GI2(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
206	GI2(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
207	GI1(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
208	GI1(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	GI1(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
210	GI1(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
211	GI1(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
212	GI1(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	GI1(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
214	GI1(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
215	VTT	--	--	--	--	--	--	--	--
216	VCC	--	--	--	--	--	--	--	--
217	GI1(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	GI1(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
219	GI1(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
220	GI1(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
221	GI1(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
222	GI1(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	GI1(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
224	GI1(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
225	GCLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
226	GCLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	GI0(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	GI0(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	GI0(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	GI0(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
231	GI0(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	GI0(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VTT	--	--	--	--	--	--	--	--
234	VCC	--	--	--	--	--	--	--	--
235	GI0(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
236	GI0(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
237	GI0(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
238	GI0(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
239	GI0(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
240	GI0(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
241	GI0(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for COMM1 VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
242	GI0(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
243	GI0(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
244	GI0(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
245	GI0(16)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
246	GI0(17)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
247	GI0(18)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
248	GI0(19)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
249	GI0(20)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
250	GI0(21)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
251	VTT	--	--	--	--	--	--	--	--
252	VCC	--	--	--	--	--	--	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	GSTALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
255	GSTALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
256	GSTALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on COMM1-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP006 - MT1. The input voltage range for this test shall be:

GaAs Inputs (For VTT = -1.8 V, V_{IH} = -0.6 V and V_{IL} = -1.7 V) (For VTT = -2.0 V V_{IH} = -0.7 V and V_{IL} = -1.9 V),. (For VTT = -2.2 V V_{IH} = -0.8 V and V_{IL} = -2.1 V),

TTL inputs (For all values of VCC, V_{IH} TTL = 4.0 and V_{IL} TTL = 0.0 V.).

1. TPLH1 -- This parameter measures the propagation delay from a TTL input directly to a Martin Marietta GaAs output. No intervening logic is present between the TI1(1:0) and GO1(1:0) pins. The propagation delay is measured from TI(0) to GO1(0). This measures the two I/O cells and a typical amount of route capacitance. The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures the time needed to generate the 10 Mhz TTL clock from the 40 MHz TTL input clock. The falling edge of the TCLK40 signal is used to generate the TCLK10 output. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures the time needed to produce the GCMP signal from a change in data input. This data is bit by bit compared for equality to a pre-stored value. The change in data values is not dependent upon bit position. This circuit is used to produce the 'Stop on Address' signal for processor run control. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- This parameter measures the time needed to produce the Serial Data Out signal from the clock edge. There are two shift chains on board the COMM1. This measurement passes through register which maintains a copy of the Internal Source and Destination busses. The alternate path passes through the register which holds the 'Stop on Adress' value. Regardless, both paths exit through the same multiplexer. The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures the time needed to produce the GERR signal from the clock edge. This signal produces a 1 cycle condition code that reflects whether there were any memory access errors. If there were, this condition code is present for the one cycle that occurs after the processor resumes execution. The rising edge of the clock produces the GERR output. The maximum acceptable value for this parameter is TBD nS.

Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

TABLE 5-2 AC Parametrics for COMM1 VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
30	TPLH1	1250	GO1(0)	TI1(0), 103	TBD
159	TPLH2	26	TCLK10	TCLK40 ↓, 113	TBD
174	TPLH3	2426	GCMP	GI0(7), 236	TBD
178	TPLH4	6674	GDSO	CLK,CLKN, 225, 226	TBD
165	TPLH5	11689	GERR	CLK, CLKN, 225, 226	TBD
30	TPHL1	1272	GO1(0)	TI1(0), 103	TBD
159	TPHL2	34	TCLK10	TCLK40 ↓, 113	TBD
174	TPHL3	1482	GCMP	GI0(7), 236	TBD
178	TPHL4	6678	GSDO	CLK,CLKN, 225, 226	TBD
165	TPHL5	11693	GERR	CLK, CLKN, 225, 226	TBD

6. APPENDIX B -- COMM1 VLSI Burn-In Circuit

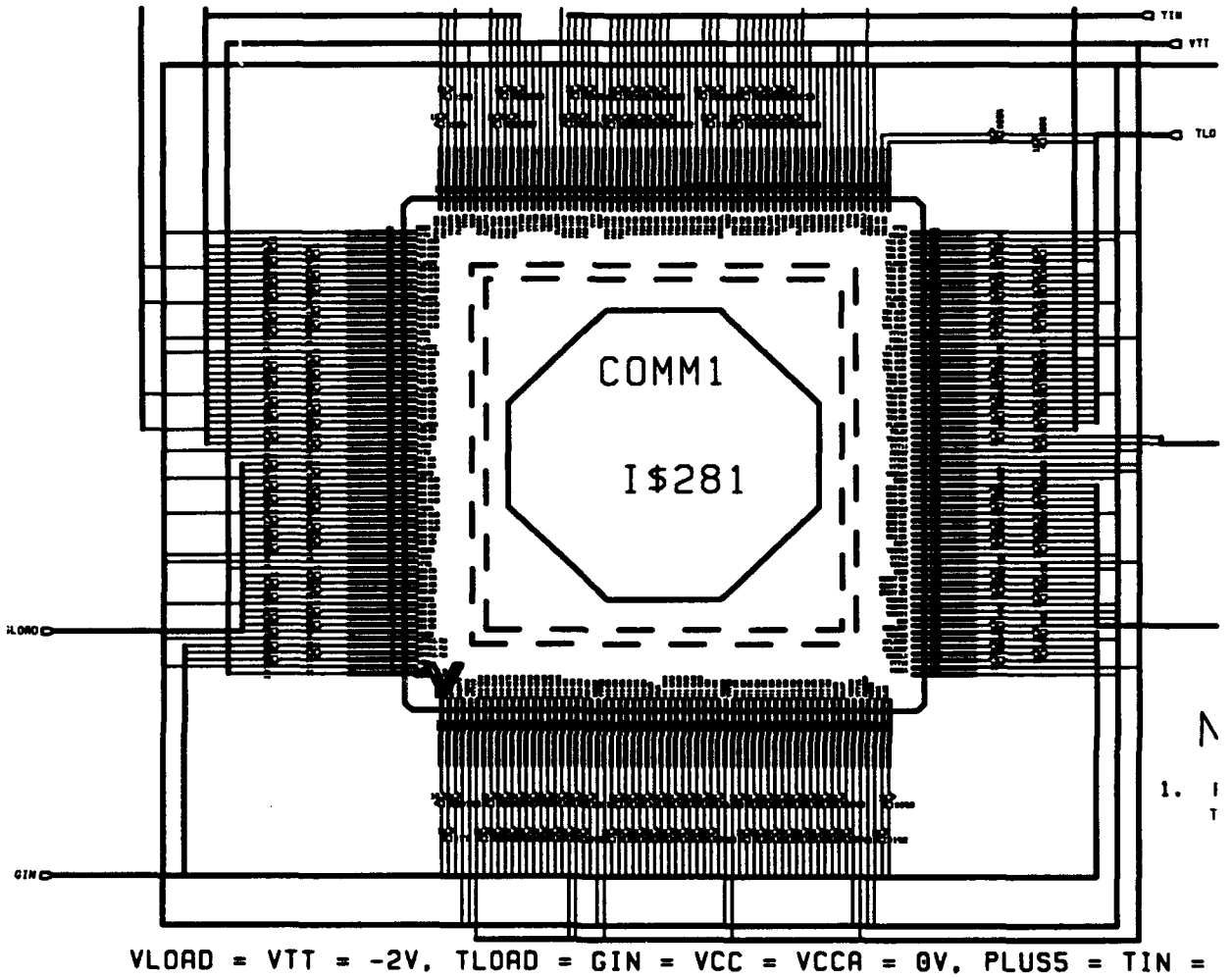

Figure 6-1 COMM1 VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- COMM1 VLSI Test Data Specification

All parametric data recorded on the COMM1 VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.

Drawing Number: GOBP007

MMSS Dash	MFG Code	Name	Address
-1		Vitesse Electronics, Inc.	841 Calle Plano Camarillo, CA. 93010
-2			

NOTES:

1. Sheet 0 shall not be furnished to supplier.
2. The 'Dash 2' configuration refers to the initial wafer run for design characterization only.
3. Only the items listed on this drawing have been evaluated and approved by Martin Marietta for use in the intended application. A substitute item shall not be used without prior evaluation and approval by Martin Marietta and the contracting organization.

PROGRAM AUTHORIZATION
Insertion Demonstrations of Digital Gallium Arsenide

MARTIN MARIETTA CORPORATION
Denver Division, P. O. Box 179, Denver Colorado,80201

Program Manager

Integrated Circuits Lead Engineer

Architecture Design Lead Engineer
John R. Meadows

Principal Design Engineer

Full Custom Microcode Sequencer for GaAs OBP.

FSCM NO. 04236

SIZE	DRWG. NO.	REV
A	GOBP007	
SCALE	PAGE	SHEET 0 of 42

Drawing Number: GOBP007

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
	Initial Release	9/12/91	

											REV
		42	41	40	39	38	37	36	35	34	SH
											REV
33	32	31	30	29	28	27	26	25	24	23	SH
											REV
22	21	20	19	18	17	16	15	14	13	12	SH
											REV
11	10	9	8	7	6	5	4	3	2	1	SH

PROGRAM AUTHORIZATION

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SIZE	DRWG. NO.	REV
A	GOBP007	

SCALE	PAGE	SHEET
		1 of 42

Drawing Number: GOBP007

REVISIONS				
REV	SH	DESCRIPTION	DATE	APPROVED

FSCM NO. 04236

	SIZE A	DRWG. NO. GOBP007	REV
	SCALE	PAGE	SHEET 2 of 42

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1. SCOPE

1.1 General - This specification establishes the performance and testing requirements for the E/D mode MESFET full custom MCS VLSI; hereinafter referred to as GOBP007, MCS, or part.

1.2 Part Number - The GALU VLSI shall be identified by the part number GOBP007.

1.3 Absolute Maximum Ratings - The absolute maximum ratings over operating free-air temperature range shall be as follows.

Supply voltage range (V_{CC}=0), V_{TT} ..... +0.5V to -2.5V
Storage Temperature Range ..... -65C TO 150C
Continuous Output Current (-2.5V < Vout< V_{TT} < + 0.5V) ..... +/- 24 mA (any output)
Supply Current , I_{TT} ..... 3.50 A
Maximum Operating Frequency ..... 80 MHz

1.4 Operating Condition Range -

	MIN	NOM	MAX	UNIT
V_{TT} Supply Voltage (V_{CC}=V_{CCA}=0V)	-2.2	-2.0	-1.8	V
I_{TT} Operating Supply Current	+2.6	+2.8	+3.0	A
Ta Operating Free-air Temperature	-55	+60	125	deg C
Tsu Input Setup Time	-	-	0.5	nS
Th Input Hold Time	-	-	0.0	nS

2. APPLICABLE DOCUMENTS

2.1 Issues of Documents

The following documents, of the issue in effect on date of invitation for bids, unless otherwise directed by the statement of work, form part of this specification as stated herein.

2.1.1 Specifications

2.1.1.1 Military

MIL-M-38510	Microcircuits, General Specification for
MIL-STD-883B	Test Methods and Procedures for Microelectronics

2.1.1.2 Standards

2.1.1.2.1 Military

MIL-STD-129	Marking for Shipment and Storage
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.1.1.2.2 Other Documents

GOBP007-MT1	Magnetic media functional description of MCS VLSI
GOBP007-MT2	Magnetic media graphical description of MCS VLSI
GOBP007-MT3	Magnetic media assembly drawing of MCS VLSI

2.2 Order of Precedence

In the event of a conflict between the requirements of this specification and other applicable documents, the following order of precedence shall apply:

1. The subcontract statement of work.

2. This specification.

3. Other documents included by reference in this document.

3. REQUIREMENTS

3.1 General - Requirements shall be in accordance with MIL-STD-883 flow for Class B devices. The manufacturer of the MCS VLSI shall have and use production and test facility flow control and accountability procedures. A quality and reliability assurance program adequate to ensure successful compliance with the provisions of the specification shall be selected for the production flow of this device. Special handling procedures and controls shall be used for the electrostatic discharge (ESD) sensitive devices.

3.2 Item Detail Requirements - The individual requirements and the electrical characteristics for parts delivered under this specification shall be as specified in the tables of Appendix A. Unless otherwise specified, all parts shall have an operating temperature range from -55 degrees C to +125 degrees C.

3.2.1 Terminal Connections - The terminal connections shall be as specified in Figure 3-1. A GDSII representation of this drawing is contained on magnetic tape GOBP007-MT3.

3.2.2 Functional Specification - Devices procured to this specification shall pass 100% of the test patterns provided on magnetic tape GOBP007-MT1.

3.2.3 Layout Specification - Devices procured to this specification shall be fabricated from tooling constructed from the detailed physical description provided on magnetic tape GOBP007-MT2.

3.2.4 DC Characteristics - The DC operating characteristics of the MCS VLSI are as defined in the Table 5-1, DC Performance Characteristics.

3.2.5 AC Characteristics - The AC operating characteristics of the MCS VLSI are as defined in the Table 5-2, AC Performance Characteristics.

3.2.6 Radiation Resistance

The MCS VLSI shall be manufactured in a radiation resistant technology. Devices supplied to this specification should be manufactured in a 1.2 micron, E/D GaAs MESFET process. Upon request, the vendor shall permit on site examination of process flow documentation for the purposes of determining process impact on device radiation hardness. Martin Marietta has performed the design of the MCS VLSI such that a device fabricated in the above mentioned process will exhibit the following characteristics:

3.2.6.1 Total Dose - Exposure to 3E4 rads (Si) total dose and exhibit no electrical degradation beyond the parametric limits specified in Appendix A.

3.2.6.2 Latch Up - Exposure to a 3e-7 sec pulse of ionizing radiation at a dose rate of 1e11 rad/sec and not exhibit sustained latchup.

3.2.6.3 Single Particle Upset - Exposure to a 1e-6 second pulse of ionizing radiation at a dose rate of 1e3 rad/sec and not exhibit data loss from critical storage elements.

The above characteristics have been demonstrated on a device test vehicle representative of the technology. This specification does not require re-characterization explicitly for the MCS VLSI.

3.3 Process-conditioning, Testing, and Screening - Process-conditioning, testing and screening shall be as specified in Section 4.4.2 which specifies the flow of MIL-STD-883, Method 5004 tests, with the exception of Salt Spray.

3.4 Marking

3.4.1 Package Marking - Devices procured to this specification shall exhibit package marking as follows:

a. The manufacturer's name,

b. Martin Marietta Corporation part number GOBP007-1,

c. The inspection lot identification and date code,

d. An index tab or other indicator marking the starting point for the number of leads,

e. Manufacturers identification, and

f. Serialization per MIL-M-38510, Para. 3.6.

The country of origin shall be retained on the initial container. This marking shall specify USA as the country of origin.

Prototype devices made for the purposes of design characterization shall be marked as above except that the Martin Marietta Corporation part number shall be changed to GOBP007-2.

3.5 Bonding System - The internal lead wire shall be monometallic with respect to the die metallization.

3.6 Traceability - Traceability to the wafer lot shall be a requirement of this specification. Inspection lot records shall be maintained to provide traceability to the serial number assigned at Initial Electricals to the specific wafer lot from which the die originated.

3.7 Design and Construction - The MCS VLSI shall be packaged in a 344 pin, hermetically sealed, leaded carrier. The package shall be of 'cavity up' orientation, and shall have a Cu-W heat spreader attached to the case floor. The physical dimensions of the package shall be as specified in Figure 3-1 of this document and magnetic tape GOBP007-MT3.

3.7.1 Burn-In and Qualification Test Circuit - Devices procured to this specification, and requiring either burn-in or lot qualification shall be biased according to the circuit specified in Appendix B.

Figure 3-1 Packaging Requirements

4. PRODUCT ASSURANCE PROVISIONS

4.1 General - Product assurance includes all inspections, analyses, physical compatibility verifications and tests deemed necessary to determine that the product presented for acceptance is in compliance with the requirements of this specification.

4.2 Quality Conformance Inspection - Quality conformance specification shall be in accordance with MIL-STD-883 Method 5005.10.

4.2.1 Wafer Probe - Each part shall be subjected to a functional test using the test vectors specified on magnetic tape GOBP007-MT1 at wafer probe. These vectors shall be applied at a frequency not less than 1e6 cycles/sec.

4.3 Vector Test - Devices procured to this specification shall pass 100% of the test vectors specified on magnetic tape GOBP007-MT1 at final package test. These vectors shall be applied at a frequency not less than 1e7 cycles/sec. Functional testing will be done with the tester providing an active current load of 1.6 mA for Output Low and -1.6 mA for Output High.

4.4 Microcircuit Qualification - Devices shall be manufactured in accordance with MIL-STD-883 Method 5005.10 lot acceptance requirements.

4.4.1 Test Data - All electrical, and parametric screening data obtained during initial electricals (at 25 °C only) and at final electricals (at 25 °C only) shall be supplied to Martin Marietta. Also, the results of all failure analysis work shall be documented and supplied to Martin Marietta.

4.4.2 Microcircuit Screening and Qualification Method - The manufacturer shall provide screening and qualification of MCS VLSI according to the following steps:

1. Internal Visual Inspection - In accordance with MIL-STD-883, Method 5004, paragraph 3.3.1a.

2. Backside Symbolization - Devices shall be symbolized as required per paragraph 3.4.1 of this document.

3. Stabilization Bake - In accordance with MIL-STD-883, Method 1008; condition C ; 24 hour minimum and 150 degree C max.

4. Temperature cycle - In accordance with MIL-STD-883 Method 1010, condition C.

5. Constant Acceleration - In accordance with MIL-STD-883, Method 2001, Condition E, Y1 only.

6. Preburn-In Test - Tests and limits will be in conformance with the DC and AC specification contained in Appendix A.

7. Burn-in - In accordance with MIL-STD-883, Condition A, for 160 hour minimum at 125 degrees C. Burn-in should be performed in accordance with the attached Burn-in diagram in Appendix B.

8. Final Electrical Test - -55 °C, +125 °C, and 25 °C per data in Appendix A.

9. Seal Test - In accordance with MIL-STD-883, Method 1014.

   a. Fine leak - Condition B with a limit of $5x10^{-8}$ cc/sec.

   b. Condition C.

10. Group A Inspection - In accordance with MIL-STD-883, Method 5005 for Class B devices. The following subgroups shall be completed.

    a. Quality Conformance Inspection - Group A per MIL-STD-883, Method 5005, Class B.

    b. Static.

       i. 25 °C, Subgroup 1.

       ii. -55 °C, +125 °C, Subgroups 2 & 3.

    c. Dynamic, 25 °C, Subgroup 9.

    d. Functional, 25 °C, Subgroup 7.

    e. Groups B & C, per MIL-STD-883, Method 5005.

    f. Group D, per MIL-STD-883, Method 5005, except Subgroup 5.

5. APPENDIX A -- Electrical Operating Characteristics

5.1 DC Operating Characteristics

The following parameters have been defined for the power pins on MCS-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. ICCL -- The Power Supply Current test with a dominant number of input and output states LOW. The device should be subjected to test patterns 1 - 7. The pattern drivers should be connected, and forcing pattern number 7. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCL_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = VCCA = VCC = 0 V.

2. ICCH -- The Power Supply Current test with a dominant number of input and output states HIGH. The device should be subjected to test patterns 1 - 11,300. The patterns drivers should be connected, and forcing pattern number 11,300. A one millisecond dwell time shall be set prior to performing the measurement. Pass criteria shall be $ICCH_{MAX}$ = +3.0 Amperes when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

The following parameters have been defined for the input pins on MCS-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum.

1. VIH -- The Input High voltage. Pass criteria shall be VIH_{MIN} = - 0.7 Vwhen the test is performed with the following parametric conditions:

   VTT = -2.0 V, VCCA = VCC = 0 V.

2. VIH ECL 100K -- The ECL Input High voltage. Pass criteria shall be VIH_{MIN} = -1.2V

3. VIL -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.9 V when the test is performed with the following parametric conditions:

   VTT = -2.0 V, VCCA = VCC = 0 V.

4. VIL ECL 100K -- The Input Low Voltage. Pass criteria shall be VIL_{MAX} = -1.5 V

5. IIH -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

6. IIH ECL 100K -- The Input HIGH State Leakage Current test. Pass criteria shall be IIH_{MAX} = -5.0 mA when the test is performed with the following parametric conditions:

   VTT = -2.1 V, VIN = -0.4 V, VCCA = VCC = 0 V.

7. IIL -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

8. IIL ECL 100K -- The Input LOW State Leakage Current test. Pass Criteria shall be IIL_{MAX} = +400 uA when the test is performed with the following parametric conditions:

   VIN = VTT = -2.1 V, VCCA = VCC = 0 V.

9. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

10. VCD1N ECL 100K -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8 V when the test is performed with the following parametric conditions

    IOL = -3 mA, VTT = VCCA = VCC = 0 V.

11. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

12. VCD1P ECL 100K -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

    IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

The following parametric tests are defined for the output pins on MCS-VLSI. Devices procured to this specification shall have no other parametric tests performed upon them.

1. VOL -- The Output LOW State Voltage test. Pass criteria shall be VOL_{MAX} = -1.7 V when the test is performed with the following parametric conditions:

   IOL = +1.6 mA into the device pin, VTT = -1.8 V, VCCA = VCC = 0 V, R_{TERM} = 50 Ohms to VTT.

2. VOL ECL 100K -- The Output LOW State Voltage test. Pass cirteria shall be VOL_{MAX} = -1.6V when the test is performed with the following parametric conditions: R_{load}=50 Ohm to VTT, VTT = -1.9 V, VCCA = VCC = 0 V.

3. VOH -- The Output HIGH State Voltage test. Pass criteria shall be VOH_{min} = -0.9 V when the test is performed with the following parametric conditions:

   IOH = -1.6 mA into the device pin, VTT = -2.2 V, VCCA = VCC = 0 V, R_{TERM} = 50 Ohms to VTT..

4. VOH ECL 100K -- The Output HIGH State Voltage test. Pass cirteria shall be VOH_{Min} = -0.6V when the test is performed with the following parametric conditions: R_{load}=50 Ohm to VTT, VTT = -2.1 V, VCCA = VCC = 0 V.

5. VCD1N -- The Negative Current ESD Clamp Diode Voltage test. Pass criteria shall be $VCD1N_{MIN}$ = -0.8V when the test is performed with the following parametric conditions:

   IOL = -3 mA, VTT = VCCA = VCC = 0 V.

6. VCD1P -- The Positive Current Termination Diode Voltage test. Pass criteria shall be $VCD1P_{MAX}$ = +2.0 V when the test is performed with the following parametric conditions:

   IOH = +3.0 mA, VTT = VCCA = VCC = 0 V.

7. IOSH -- The Output HIGH State Short Circuit Current Source test. Pass criteria shall be $IOSH_{MIN}$ = -10 mA when the test is performed with the following parametric conditions:

   VOL = VTT = -1.9 V, VCCA = VCC = 0 V.

8. IOSL -- The Output LOW State Short Circuit Current Sinking test. Pass criteria shall be $IOSL_{MIN}$ = +10 mA when the test is performed with the following parametric

conditions:

VTT = -1.9 V, VOH = -0.6 V, VCCA = VCC = 0 V.

In Table 5-1, the pins are listed sequentially from 1 to 344, forming the table row entries. The DC parametric tests are shown as the table columns. Where a parametric measurement is to be made, the test vector which defines the state of the device for the test is shown. Where the corresponding test has no meaning , two dashes are shown.

TABLE 5-1 DC Parametrics for MCS VLSI

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
1	VCC	--	--	--	--	--	--	--	--
2	VCCA	--	--	--	--	--	--	--	--
3	VCC	--	--	--	--	--	--	--	--
4	VTT	--	--	--	--	--	--	--	--
5	STALL(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
6	STALL(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
7	STALL(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
8	STALL(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
9	STALL(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
10	STALL(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
11	MSLD	--	--	Note 1	Note 1	--	--	Note 1	Note 1
12	MSSEL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
13	PIPGO	--	--	Note 1	Note 1	--	--	Note 1	Note 1
14	SSEL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
15	FCONT	--	--	Note 1	Note 1	--	--	Note 1	Note 1
16	SDOSEL	--	--	Note 1	Note 1	--	--	Note 1	Note 1
17	VCC	--	--	--	--	--	--	--	--
18	VTT	--	--	--	--	--	--	--	--
19	CTF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
20	CCS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
21	CCS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
22	CCS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
23	CCS(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
24	CCS(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
25	SQI(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
26	SQI(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
27	SQI(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
28	SQI(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
29	DBD(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
30	DBD(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
31	DBD(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
32	VCC	--	--	--	--	--	--	--	--
33	VTT	--	--	--	--	--	--	--	--
34	DBD(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
35	DBD(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
36	SBS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
37	SBS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
38	SBS(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
39	SBS(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
40	SBS(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
41	BAS(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
42	BAS(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
43	BAI(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
44	BAI(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
45	BAI(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
46	BAI(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
47	VCC	--	--	--	--	--	--	--	--
48	VTT	--	--	--	--	--	--	--	--
49	BAI(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
50	BAI(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
51	BAI(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
52	BAI(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
53	BAI(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
54	BAI(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
55	BAI(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
56	BAI(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
57	BAI(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
58	BAI(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
59	BAI(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
60	BAI(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
61	VCC	--	--	--	--	--	--	--	--
62	VTT	--	--	--	--	--	--	--	--
63	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
64	VCCA	--	--	--	--	--	--	--	--
65	CSF(3) ECL OUTPUT	20	16	Note 1	Note 1	16	20	--	--
66	CSF(2) ECL OUTPUT	168	176	Note 1	Note 1	176	168	--	--
67	CSF(1) ECL OUTPUT	160	168	Note 1	Note 1	168	160	--	--
68	CSF(0) ECL OUTPUT	152	160	Note 1	Note 1	160	152	--	--
69	VCCA	--	--	--	--	--	--	--	--
70	FARE(15) ECL OUTPUT	144	136	Note 1	Note 1	136	144	--	--
71	FARG(15)	144	136	Note 1	Note 1	136	144	--	--
72	FARE(14) ECL OUTPUT	136	128	Note 1	Note 1	128	136	--	--
73	FARG(14)	136	128	Note 1	Note 1	128	136	--	--
74	VCCA	--	--	--	--	--	--	--	--
75	FARE(13) ECL OUTPUT	128	120	Note 1	Note 1	120	128	--	--
76	VCC	--	--	--	--	--	--	--	--
77	VTT	--	--	--	--	--	--	--	--
78	FARG(13)	128	120	Note 1	Note 1	120	128	--	--
79	FARE(12) ECL OUTPUT	120	112	Note 1	Note 1	112	120	--	--
80	FARG(12)	120	112	Note 1	Note 1	112	120	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
81	VCCA	--	--	--	--	--	--	--	--
82	FARE(11) ECL OUTPUT	112	104	Note 1	Note 1	104	112	--	--
83	FARG(11)	112	104	Note 1	Note 1	104	112	--	--
84	FARE(10) ECL OUTPUT	104	96	Note 1	Note 1	96	104	--	--
85	FARG(10)	104	96	Note 1	Note 1	96	104	--	--
86	VCCA	--	--	--	--	--	--	--	--
87	FARE(9) ECL OUTPUT	96	88	Note 1	Note 1	88	96	--	--
88	FARG(9)	96	88	Note 1	Note 1	88	96	--	--
89	FARE(8) ECL OUTPUT	88	80	Note 1	Note 1	80	88	--	--
90	VCC	--	--	--	--	--	--	--	--
91	VTT	--	--	--	--	--	--	--	--
92	FARG(8)	88	80	Note 1	Note 1	80	88	--	--
93	VCCA	--	--	--	--	--	--	--	--
94	FARE(7) ECL OUTPUT	80	72	Note 1	Note 1	72	80	--	--
95	FARG(7)	80	72	Note 1	Note 1	72	80	--	--
96	FARE(6) ECL OUTPUT	72	64	Note 1	Note 1	64	72	--	--
97	FARG(6)	72	64	Note 1	Note 1	64	72	--	--
98	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
99	FARE(5) ECL OUTPUT	64	56	Note 1	Note 1	56	64	--	--
100	FARG(5)	64	56	Note 1	Note 1	56	64	--	--
101	FARE(4) ECL OUTPUT	56	48	Note 1	Note 1	48	56	--	--
102	FARG(4)	56	48	Note 1	Note 1	48	56	--	--
103	VCCA	--	--	--	--	--	--	--	--
104	VCC	--	--	--	--	--	--	--	--
105	VTT	--	--	--	--	--	--	--	--
106	FARE(3) ECL OUTPUT	48	40	Note 1	Note 1	40	48	--	--
107	FARG(3)	48	40	Note 1	Note 1	40	48	--	--
108	FARE(2) ECL OUTPUT	40	32	Note 1	Note 1	32	40	--	--
109	FARG(2)	40	32	Note 1	Note 1	32	40	--	--
110	VCCA	--	--	--	--	--	--	--	--
111	FARE(1) ECL OUTPUT	32	20	Note 1	Note 1	20	32	--	--
112	FARG(1)	32	20	Note 1	Note 1	20	32	--	--
113	FARE(0) ECL OUTPUT	20	16	Note 1	Note 1	16	20	--	--
114	FARG(0)	20	16	Note 1	Note 1	16	20	--	--
115	VCCA	--	--	--	--	--	--	--	--
116	BRAN(15)	141	133	Note 1	Note 1	133	141	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
117	BRAN(14)	133	125	Note 1	Note 1	125	133	--	--
118	VCC	--	--	--	--	--	--	--	--
119	VTT	--	--	--	--	--	--	--	--
120	BRAN(13)	125	117	Note 1	Note 1	117	125	--	--
121	BRAN(12)	117	109	Note 1	Note 1	109	117	--	--
122	VCCA	--	--	--	--	--	--	--	--
123	BRAN(11)	109	101	Note 1	Note 1	101	109	--	--
124	BRAN(10)	101	93	Note 1	Note 1	93	101	--	--
125	CLKN	--	--	Note 1	Note 1	--	--	Note 1	Note 1
126	CLK	--	--	Note 1	Note 1	--	--	Note 1	Note 1
127	VCCA	--	--	--	--	--	--	--	--
128	BRAN(9,	93	85	Note 1	Note 1	85	93	--	--
129	BRAN(8)	85	77	Note 1	Note 1	77	85	--	--
130	BRAN(7)	77	69	Note 1	Note 1	69	77	--	--
131	BRAN(6)	69	61	Note 1	Note 1	61	69	--	--
132	VCC	--	--	--	--	--	--	--	--
133	VTT	--	--	--	--	--	--	--	--
134	VCCA	--	--	--	--	--	--	--	--
135	BRAN(5)	61	53	Note 1	Note 1	53	61	--	--
136	BRAN(4)	53	45	Note 1	Note 1	45	53	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
137	BRAN(3)	45	37	Note 1	Note 1	37	45	--	--
138	BRAN(2)	37	29	Note 1	Note 1	29	37	--	--
139	VCCA	--	--	--	--	--	--	--	--
140	BRAN(1)	29	21	Note 1	Note 1	21	29	--	--
141	BRAN(0)	21	13	Note 1	Note 1	13	21	--	--
142	INTREQ	448	440	Note 1	Note 1	440	448	--	--
143	INTACT	464	448	Note 1	Note 1	448	464	--	--
144	VCCA	--	--	--	--	--	--	--	--
145	BF	473	469	Note 1	Note 1	469	473	--	--
146	VCC	--	--	--	--	--	--	--	--
147	VTT	--	--	--	--	--	--	--	--
148	CCODE	537	573	Note 1	Note 1	573	537	--	--
149	SDO	144	136	Note 1	Note 1	136	144	--	--
150	BP	--	--	Note 1	Note 1	--	--	Note 1	Note 1
151	VCCA	--	--	--	--	--	--	--	--
152	IENF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
153	IRQ(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
154	IRQ(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
155	IRQ(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
156	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
157	IRQ(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
158	IRQ(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
159	IRQ(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
160	VCC	--	--	--	--	--	--	--	--
161	VTT	--	--	--	--	--	--	--	--
162	IRQ(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
163	VCCA	--	--	--	--	--	--	--	--
164	IRQ(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
165	IRQ(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
166	IRQ(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
167	IRQ(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
168	VCCA	--	--	--	--	--	--	--	--
169	IRQ(2)	--	--	--	--	--	--	--	--
170	IRQ(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
171	IRQ(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
172	VCC	--	--	--	--	--	--	--	--
173	VCC	--	--	--	--	--	--	--	--
174	VCCA	--	--	--	--	--	--	--	--
175	VCC	--	--	--	--	--	--	--	--
176	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
177	DEST(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
178	DEST(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
179	DEST(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
180	DEST(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
181	DEST(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
182	DEST(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
183	DEST(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
184	DEST(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
185	DEST(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
186	DEST(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
187	DEST(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
188	DEST(4)	--	--	Note 1	Note 1			Note 1	Note 1
189	VCC	--	--	--	--	--	--	--	--
190	VTT	--	--	--	--	--	--	--	--
191	DEST(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
192	DEST(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
193	DEST(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
194	DEST(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
195	CC(28)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
196	CC(27)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
197	CC(26)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
198	CC(25)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
199	CC(24)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
200	CC(23)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
201	CC(22)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
202	CC(21)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
203	CC(20)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
204	VCC	--	--	--	--	--	--	--	--
205	VTT	--	--	--	--	--	--	--	--
206	CC(19)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
207	CC(18)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
208	CC(17)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
209	CC(16)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
210	CC(15)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
211	CC(14)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
212	CC(13)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
213	CC(12)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
214	CC(11)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
215	CC(10)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
216	CC(9)	--	--	Note 1	Note 1	--	--	Note 1	Note 1

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
217	CC(8)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
218	CC(7)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
219	VCC	--	--	--	--	--	--	--	--
220	VTT	--	--	--	--	--	--	--	--
221	CC(6)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
222	CC(5)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
223	CC(4)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
224	CC(3)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
225	CC(2)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
226	CC(1)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
227	CC(0)	--	--	Note 1	Note 1	--	--	Note 1	Note 1
228	TST	--	--	Note 1	Note 1	--	--	Note 1	Note 1
229	TSTECC	--	--	Note 1	Note 1	--	--	Note 1	Note 1
230	SCRUB	--	--	Note 1	Note 1	--	--	Note 1	Note 1
231	INITF	--	--	Note 1	Note 1	--	--	Note 1	Note 1
232	SDI	--	--	Note 1	Note 1	--	--	Note 1	Note 1
233	VCC	--	--	--	--	--	--	--	--
234	VTT	--	--	--	--	--	--	--	--
235	VCCA	--	--	--	--	--	--	--	--
236	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCD1P	IOSH	IOSL	IIH	IIL
237	VCC	--	--	--	--	--	--	--	--
238	VCC	--	--	--	--	--	--		--
239	VTT	--	--	--	--	--	--	--	--
240	VTT	--	--	--	--	--	--	--	--
241	VCCA	--	--	--	--	--	--	--	--
242	VTT	--	--	--	--	--	--	--	--
243	VTT	--	--	--	--	--	--	--	--
244	VCC	--	--	--	--	--	--	--	--
245	VCC	--	--	--	--	--	--	--	--
246	VCCA	--	--	--	--	--	--	--	--
247	VCC	--	--	--	--	--	--	--	--
248	VCC	--	--	--	--	--	--	--	--
249	VTT	--	--	--	--	--	--	--	--
250	VCC	--	--	--	--	--	--	--	--
251	VTT	--	--	--	--	--	--	--	--
252	VTT	--	--	--	--	--	--	--	--
253	VCCA	--	--	--	--	--	--	--	--
254	VTT	--	--	--	--	--	--	--	--
255	VTT	--	--	--	--	--	--	--	--
256	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
257	VTT	--	--	--	--	--	--	--	--
258	VCCA	--	--	--	--	--	--	--	--
259	VTT	--	--	--	--	--	--	--	--
260	VTT	--	--	--	--	--	--	--	--
261	VCC	--	--	--	--	--	--	--	--
262	VCC	--	--	--	--	--	--	--	--
263	VTT	--	--	--	--	--	--	--	--
264	VCC	--	--	--	--	--	--	--	--
265	VCCA	--	--	--	--	--	--	--	--
266	VTT	--	--	--	--	--	--	--	--
267	VTT	--	--	--	--	--	--	--	--
268	VTT	--	--	--	--	--	--	--	--
269	VTT	--	--	--	--	--	--	--	--
270	VCCA	--	--	--	--	--	--	--	--
271	VTT	--	--	--	--	--	--	--	--
272	VTT	--	--	--	--	--	--	--	--
273	VTT	--	--	--	--	--	--	--	--
274	VTT	--	--	--	--	--	--	--	--
275	VCCA	--	--	--	--	--	--	--	--
276	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
277	VTT	--	--	--	--	--	--	--	--
278	VCC	--	--	--	--	--	--	--	--
279	VCC	--	--	--	--	--	--	--	--
280	VCC	--	--	--	--	--	--	--	--
281	VCC	--	--	--	--	--	--	--	--
282	VCCA	--	--	--	--	--	--	--	--
283	VTT	--	--	--	--	--	--	--	--
284	VTT	--	--	--	--	--	--	--	--
285	VTT	--	--	--	--	--	--	--	--
286	VTT	--	--	--	--	--	--	--	--
287	VCCA	--	--	--	--	--	--	--	--
288	VCC	--	--	--	--	--	--	--	--
289	VCC	--	--	--	--	--	--	--	--
290	VCC	--	--	--	--	--	--	--	--
291	SEAL RING VTT	--	--	--	--	--	--	--	--
292	VCC	--	--	--	--	--	--	--	--
293	VCC	--	--	--	--	--	--	--	--
294	VCCA	--	--	--	--	--	--	--	--
295	VTT	--	--	--	--	--	--	--	--
296	VTT	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
297	VTT	--	--	--	--	--	--	--	--
298	VTT	--	--	--	--	--	--	--	--
299	VCCA	--	--	--	--	--	--	--	--
300	VCC	--	--	--	--	--	--	--	--
301	VCC	--	--	--	--	--	--	--	--
302	VCC	--	--	--	--	--	--	--	--
303	VCC	--	--	--	--	--	--	--	--
304	VCC	--	--	--	--	--	--	--	--
305	VTT	--	--	--	--	--	--	--	--
306	VCCA	--	--	--	--	--	--	--	--
307	VTT	--	--	--	--	--	--	--	--
308	VTT	--	--	--	--	--	--	--	--
309	VTT	--	--	--	--	--	--	--	--
310	VTT	--	--	--	--	--	--	--	--
311	VCCA	--	--	--	--	--	--	--	--
312	VTT	--	--	--	--	--	--	--	--
313	VTT	--	--	--	--	--	--	--	--
314	VTT	--	--	--	--	--	--	--	--
315	VTT	--	--	--	--	--	--	--	--
316	VCCA	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCD1N	VCD1P	IOSH	IOSL	IIH	IIL
317	VCC	--	--	--	--	--	--	--	--
318	VCC	--	--	--	--	--	--	--	--
319	VTT	--	--	--	--	--	--	--	--
320	VCC	--	--	--	--	--	--	--	--
321	VTT	--	--	--	--	--	--	--	--
322	VTT	--	--	--	--	--	--	--	--
323	VCCA	--	--	--	--	--	--	--	--
324	VTT	--	--	--	--	--	--	--	--
325	VTT	--	--	--	--	--	--	--	--
326	VTT	--	--	--	--	--	--	--	--
327	VTT	--	--	--	--	--	--	--	--
328	VCCA	--	--	--	--	--	--	--	--
329	VTT	--	--	--	--	--	--	--	--
330	VTT	--	--	--	--	--	--	--	--
331	VCC	--	--	--	--	--	--	--	--
332	VCC	--	--	--	--	--	--	--	--
333	VTT	--	--	--	--	--	--	--	--
334	VCC	--	--	--	--	--	--	--	--
335	VCCA	--	--	--	--	--	--	--	--
336	VCC	--	--	--	--	--	--	--	--

TABLE 5-1 DC Parametrics for MCS VLSI [continued]

PIN #	SIGNAL NAME	VOL	VOH	VCDIN	VCDIP	IOSH	IOSL	IIH	IIL
337	VCC	--	--	--	--	--	--	--	--
338	VTT	--	--	--	--	--	--	--	--
339	VTT	--	--	--	--	--	--	--	--
340	VCCA	--	--	--	--	--	--	--	--
341	VTT	--	--	--	--	--	--	--	--
342	VTT	--	--	--	--	--	--	--	--
343	VCC	--	--	--	--	--	--	--	--
344	VCC	--	--	--	--	--	--	--	--

NOTE 1 - The state of the device during test is irrelevant. The drivers and loads should be disconnected from the D.U.T. while the test is being performed.

5.2 AC PARAMETRICS

The following AC parameters are defined for the output pins on MCS-VLSI. Devices procured to this specification shall have the following parametric tests performed upon them as a minimum. The pattern number specified in Table 5-2 refers to the test vectors contained on Magnetic Tape GOBP007 - MT1. The input voltage range for this test shall be V_{IH} = -0.6 V and V_{IL} = -1.9 V.

1. TPLH1 -- This parameter measures the time to generate the condition code output from the true/false condition code select signal, CTF. This path must go only through the ccmux logic, where it inverts the already selected condition code output. This is a very short path since no decoding need to be performed. The maximum acceptable value for this parameter is TBD nS.

2. TPLH2 -- This parameter measures the time generate the FARG output bus. This is the primary address fetch path. It is registered inside the MCS VLSI. The output pin is driven directly by a change in the internal address pipeline register. Changes to this output should occur on the rising edge of the clock. The maximum acceptable value for this parameter is TBD nS.

3. TPLH3 -- This parameter measures a direct signal flow through the MCS VLSI. A change in the BAI input bus propagates through the BINTMUX and BABMUX before it reaches the BRAN bus output pins.. The maximum acceptable value for this parameter is TBD nS.

4. TPLH4 -- This parameter measures the time needed to generate the INTACT signal. This signal is generated from the registered output of the interrupt state machine controller. A change in the rising edge of the clock creates a new machine state. This machine state is decoded in a programmable logic array to determine if the MCS VLSI is entering an interrupt service routine. This parameter should reflect PLA decoding time. The maximum acceptable value for this parameter is TBD nS.

5. TPLH5 -- This parameter measures the time needed to generate a branch address from the Top of Stack register. The rising edge of the clock causes data to change on the Top of Stack register and propagate through the BABMUX to the BRAN output bus pins. The maximum acceptable value for this parameter is TBD nS.

Parameters TPHL1 - TPHL5 are the corresponding high to low transitions of TPLH1 - TPLH5. Table 5-2 summarizes these AC measurements.

TABLE 5-2 AC Parametrics for MCS VLSI

PIN #	AC TEST NAME	PATTERN OF TRANSITION	SIGNAL NAME	REFERENCE PIN, NAME	SPEC.
148	TPLH1	573	CCODE	CTF; 19	TBD
114	TPLH2	580	FARG(0)	(CLK,CLKN); 128,127	TBD
141	TPLH3	417	BRAN(0)	BAI(0); 25,23	TBD
143	TPLH4	448	INTACT	(CLK,CLKN); 128,127	TBD
129	TPLH5	8,296	BRAN(8)	(CLK,CLKN); 128,127	TBD
148	TPHL1	537	CCODE	CTF; 19	TBD
114	TPHL2	584	FARG(0)	(CLK,CLKN); 128,127	TBD
141	TPHL3	21	BRAN(0)	BAI(0); 25,23	TBD
143	TPHL4	465	INTACT	(CLK,CLKN); 128,127	TBD
129	TPHL5	8,308	BRAN(8)	(CLK,CLKN); 128,127	TBD

6. APPENDIX B -- MCS VLSI Burn-In Circuit

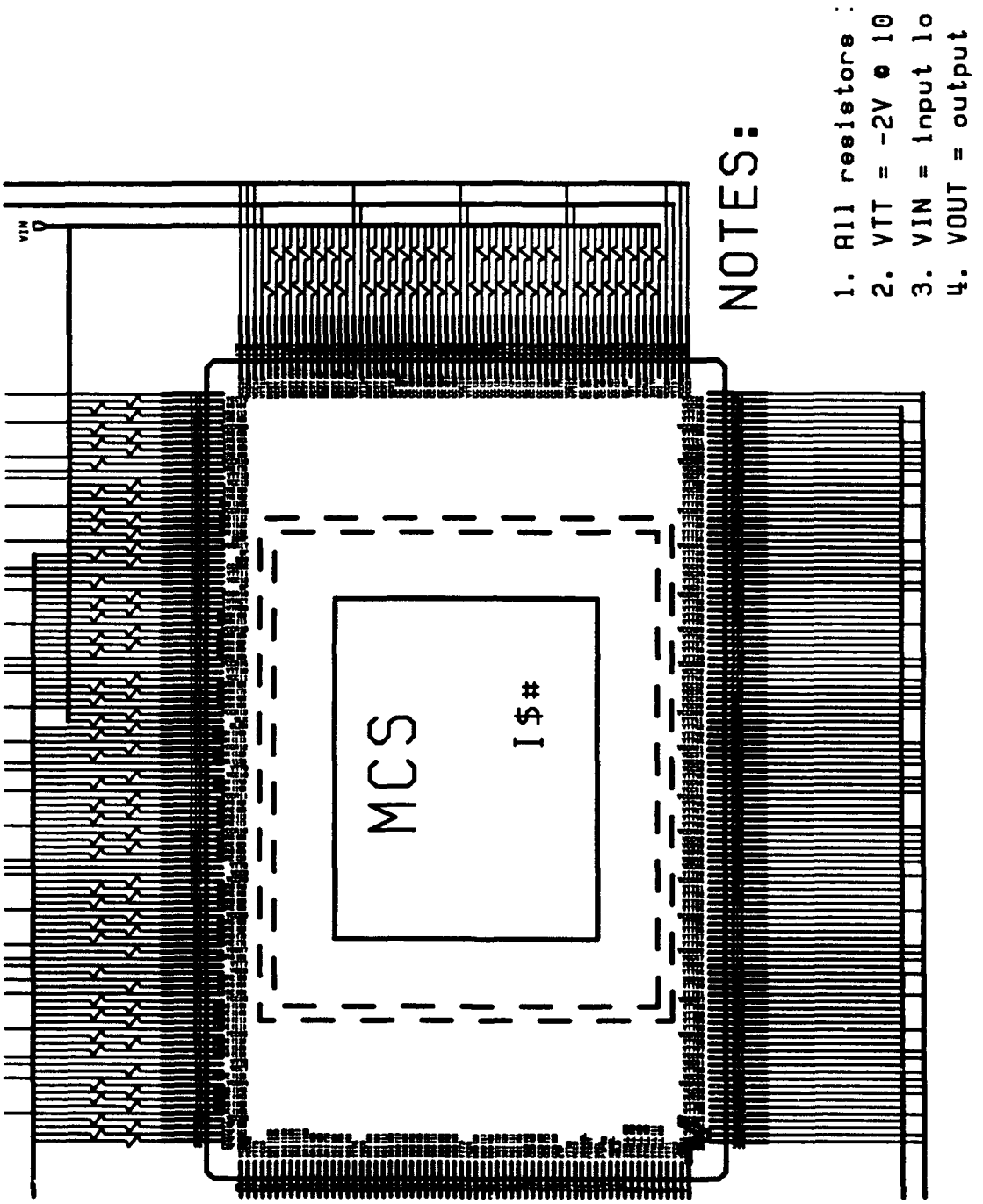

Figure 6-1 MCS VLSI Burn-In Circuit

7. APPENDIX C -- Alternate procedure for Class B Microcircuits

The following procedure should be used by the contractor as an alternate procedure for supplying a Class B microcircuit.

1. Temperature cycling (3.1.5). The minimum total number of temperature cycles shall be 50.

2. Photomask/Reticle controls must be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Critical photomask processing levels shall be non-contact.

   b. Photomask shall be serialized for all redesigns and new designs.

   c. Critical photomasks shall be inspected to a defect level not to exceed 1 defect/square cm initially and thereafter during each pellicle change procedure.

   d. Pellicles shall be used for all critical mask levels.

   e. Mask to mask registration controls shall be in place.

3. Production Process Controls shall be documented and implemented by the contractor. These controls are not limited to, but shall include the following as a minimum:

   a. Each die shall contain alignment controls. (e.g. die vernier patterns, grid keys, or adjacent control strip alignment patterns)

   b. Each wafer shall contain a test cell which shall be used for Process Control Purposes. Data shall be tracked on Process Control Charts with appropriate action limits established.

   c. SEM inspection shall be used for Process Control purposes at least once a week.

   d. There shall be Process Controls before and after photoresist etch with a documented rework cycle.

4. Records shall be maintained to show compliance to each of the requirements above.

8. APPENDIX D -- MCS VLSI Test Data Specification

All parametric data recorded on the MCS VLSI for the purposes of demonstrating compliance with the requirements of Paragraph 4.0 of this document shall be supplied to Martin Marietta on ASCII format magnetic media.

8.1 Parameter Identification - Data pertaining to each unique parameter shall be identified by a character string containing the parameter name exactly as specified in Appendix A.

8.1.1 Pin Identification - Data pertaining to a unique pin within a group of similar parametric measurements shall be identified by a character string containing the following:

A. The ASCII character string 'PIN ',

B. The pin number on which the measurement was made in the range of 1 to 256,

C. An ASCII delimitation character such as a space,

D. The value of the measurement terminated with the same delimitation character used in item C, and

E. A character string containing the units of measure.